FP5532

Low-Voltage H-Bridge Motor Driver

Description

The FP5532 provides a low-voltage H-bridge motor driver for driving brush motors, solenoids, electrical toothbrush, smart lock, gaming machines or other inductive loads.

The FP5532 fault protection includes over current limit, UVLO and thermal shutdown. In sleep mode, the supply current is about 120nA. The output can supply up to 1.8A of output current, it operates on a motor power supply voltage from 0V to 11V, and a logic power supply voltage of 1.8V to 6V.

The FP5532 has a PWM (IN1-IN2) input interface that compatible with industry-standard devices.

The FP5532 is offered in TDFN-8L (2mmx2mm) packages.

Features

- Low-Voltage H-Bridge Current Control Driver DC Motors
- Low $R_{DS(ON)}$ Integrated Power MOSFET HS+LS: 280mΩ
- Output Current Capability (At VM=5V, VCC=3V, 25°C)
  -1.8 A Peak Current
- Wide Input Voltage Range: 0V to 11V
- Low current in sleep mode: 120nA
- Input Under Voltage Lockout
- Over-Temperature Protection with Auto Recovery
- Small packages
  - TDFN-8L (2mmx2mm)

Applications

- Electrical Toothbrush
- Smart Lock
- Gaming Machines
- Robotics
- Battery-Powered Toys

Pin Assignments

D6 Package: TDFN-8L (2mmx2mm)

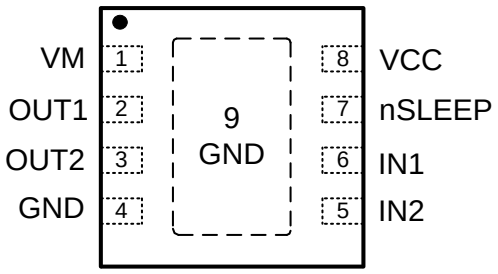


Figure 1. Pin Assignment of FP5532

Ordering Information

FP5532□

Package Type
D6: TDFN-8L (2mmx2mm)

TDFN-8L (2mmx2mm) Marking

Part Number	Product Code
FP5532D6	**GH8**

Typical Application Circuit

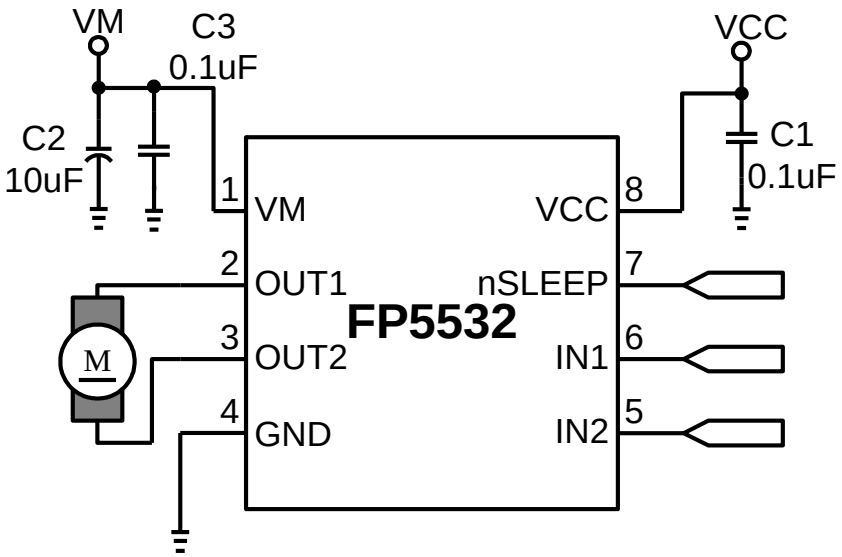


Figure 2. DC Motor Application Circuit

Functional Pin Description

Pin Name	Pin No.	I/O	Pin Function
VM	1	POWER	Motor power supply.
OUT1	2	OUTPUT	Motor output 1.
OUT2	3	OUTPUT	Motor output 2.
GND	4, 9	POWER	Ground. Connect to board ground. In order to reduce the error caused by the parasitic resistance on the board ground wire, use large ground planes on multiple layers.
IN2	5	INPUT	Input 2.
IN1	6	INPUT	Input 1.
nSLEEP	7	INPUT	Sleep mode. Logic high to enable device, logic low to enter low power sleep mode and reset all internal logic. Internal pull-down.
VCC	8	POWER	Logic power supply.

Block Diagram

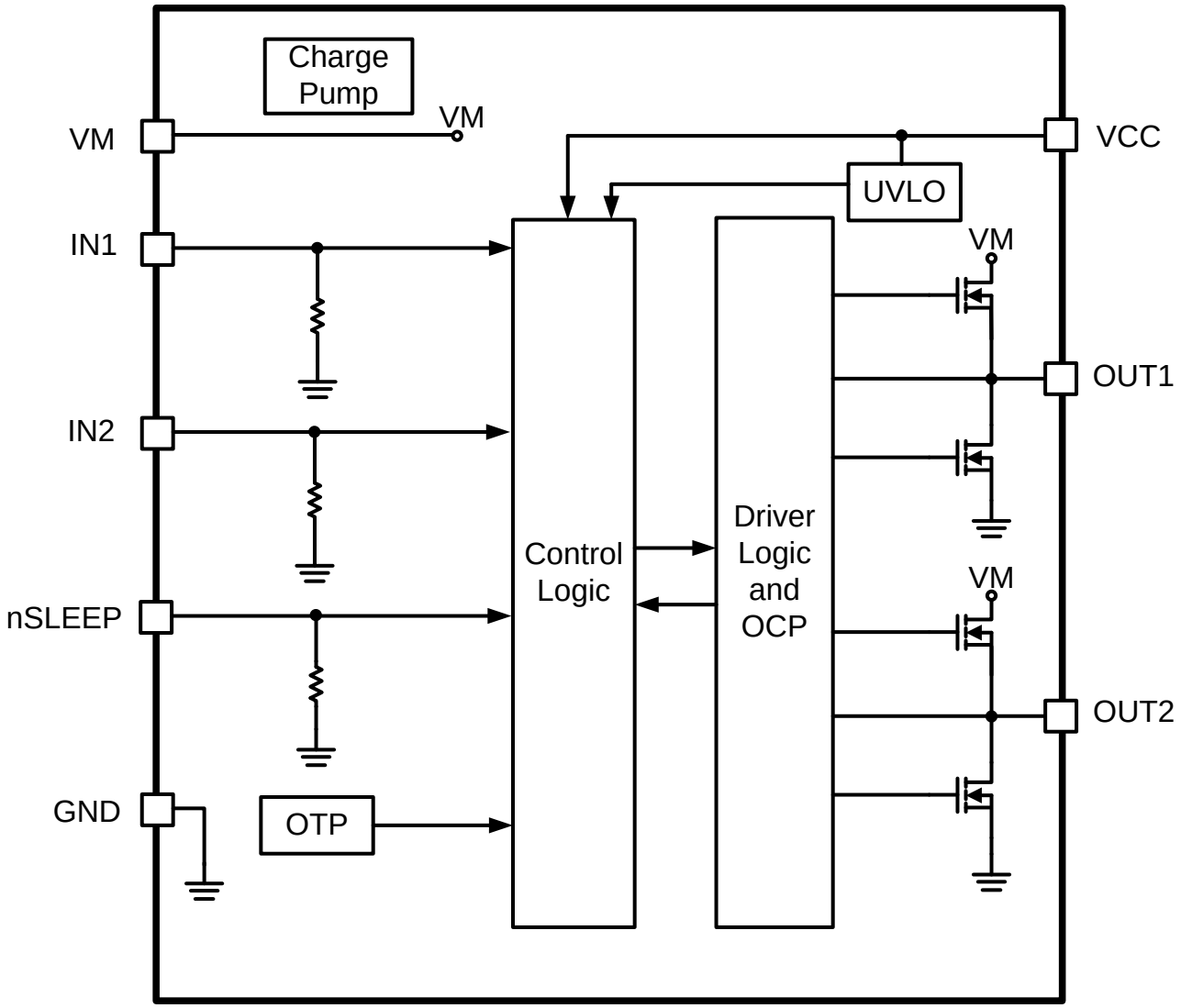


Figure 3. Block Diagram of FP5532

Absolute Maximum Ratings (Note 1)

- Motor power supply voltage range (VM) ---------- -0.3V to +12V
- Logic power supply voltage range (VCC) ---------- -0.3V to +6.5V
- Digital input pin voltage ---------- -0.3V to +6.5V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Package Thermal Resistance, (θ_{JA})
  - TDFN-8L (2mmx2mm) ---------- 90°C/W
- Package Thermal Resistance, (θ_{JC})
  - TDFN-8L (2mmx2mm) ---------- 12°C/W
- ESD
  - HBM ---------- ±4kV
  - MM ---------- ±0.3kV
  - CDM* ---------- ±1.5kV

* CDM test is based on JESD22-C101F

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Motor power supply voltage range (VM) ---------- 0 to +11V
- Logic power supply voltage range (VCC) ---------- +1.8V to +6V
- Digital input pin voltage range ---------- 0 to +6V
- Motor peak current ---------- 0 to 1.8A
- Applied PWM signal to Inx ---------- 0 to 250kHz
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

TA=25°C, over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
VM operating voltage	VM		0		11	V
VM operating supply current	I_{VM}	VM=5V, VCC=3V, INx=low, nSLEEP=H		40	100	uA
VM operating supply current	I_{VM}	VM=5V, VCC=3V, 50kHz PWM, nSLEEP=H		0.8	1.5	mA
VM sleep mode supply current	I_{VMQ}	VM=5V, VCC=3V, nSLEEP=L		30	95	nA
VCC operating voltage	VCC		1.8		6	V
VCC operating supply current	I_{VCC}	VM=5V, VCC=3V, INx=low, nSLEEP=H		300	500	uA
VCC operating supply current	I_{VCC}	VM=5V, VCC=3V, 50kHz PWM, nSLEEP=H		0.7	1.5	mA
VCC sleep mode supply current	I_{VCCQ}	VM=5V, VCC=3V, nSLEEP=L		5	25	nA
Wake up time	t_{WAKE}	nSLEEP=H to output transition		10	30	us
Logic-Level Inputs						
Input low voltage	V_{IL}	INx, nSLEEP			0.25*VCC	V
Input high voltage	V_{IH}	INx, nSLEEP	0.5*VCC			V
Input hysteresis	V_{HYS}			0.08*VCC		V
Input pulldown resistance	R_{PD}	INx, nSLEEP		100		kΩ
Input low current	I_{IL}	VIN=0V	-5		5	uA
Input high current	I_{IH}	VIN=3.3V			50	uA
Propagation delay INx to OUTx	t_{PROP}	VM=5V, VCC=3, 20Ω			160	ns
Motor Driver Outputs (OUTx)						
HS + LS FET on resistance	Rds(on)	VM=5V, VCC=3V, Io=800mA, Tj=25℃		280	330	mΩ
Off-state leakage current	IOFF	Vout=0V	-200		200	nA
Rise time	tR	VM=5V, VCC=3, 47Ω			0.5	us
Fall time	tF	VM=5V, VCC=3, 47Ω			0.5	us

Electrical Characteristics (Continued)

TA=25°C, over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Protection Circuits						
VCC under voltage lockout	V_{UVLO}	VCC falling; UVLO report			1.7	V
		VCC rising; UVLO recovery			1.8	V
Over current protection trip level	I_{OCP}		1.9		3.5	A
OCP deglitch time	t_{DEG}			1		us
Over current protection period	t_{OCP}			1		ms
Thermal shutdown temperature (Note 2)	t_{TSD}	Die temperature	150	160	180	°C
I/O Propagation Delay and Timing Requirement						
Output enable time	t_{EN}	VM=5V, VCC=3, 47Ω			0.8	us
Output disable time	t_{DIS}	VM=5V, VCC=3, 47Ω			0.8	us
Delay time, INx high to OUTx high	t_{DH}	VM=5V, VCC=3, 47Ω			0.7	us
Delay time, INx low to OUTx low	t_{DL}	VM=5V, VCC=3, 47Ω			0.7	us

Note 2: Not production tested.

Input and Output Timing

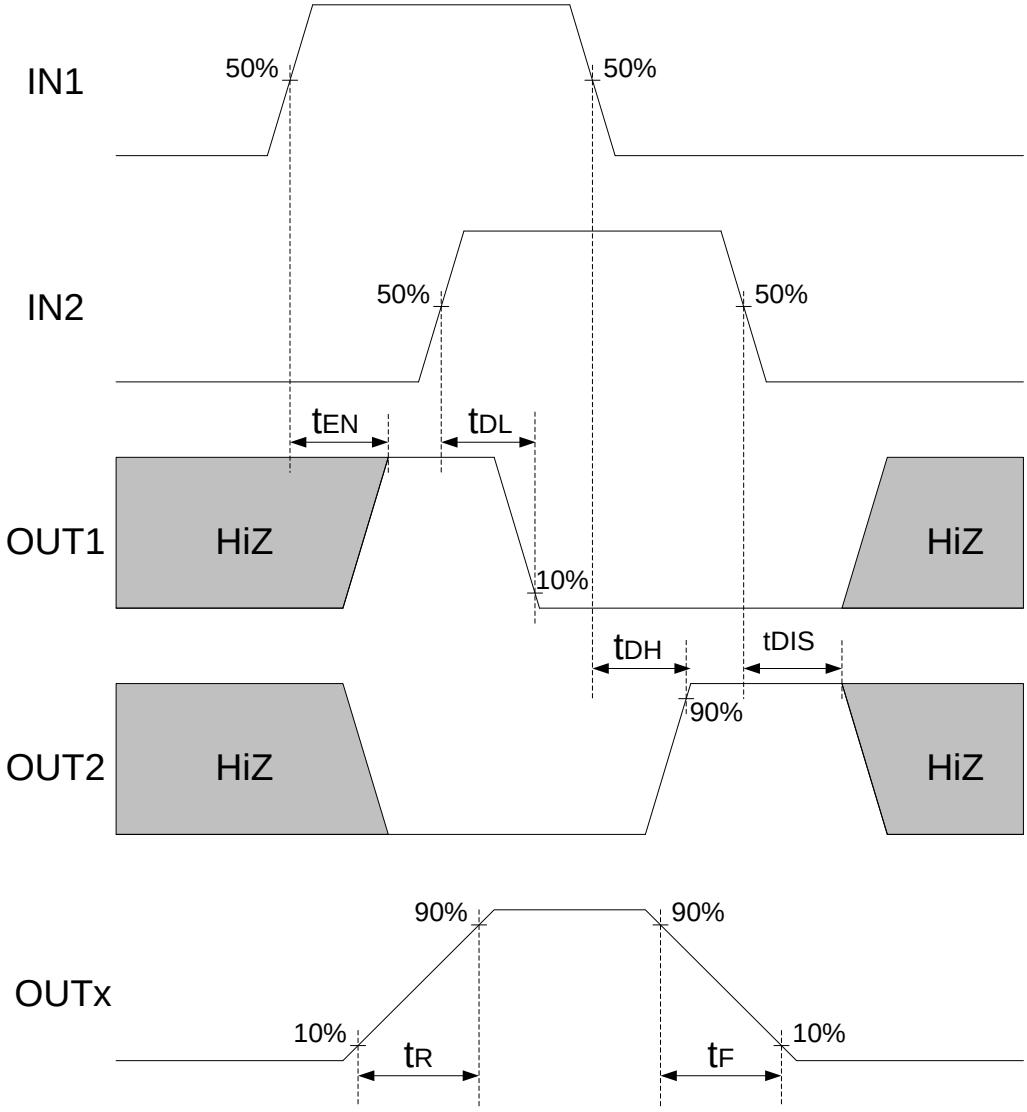


Figure 4. Input and Output Timing

Function Description

The FP5532 is a motor driver for brushed DC. The device integrated H-bridge and current regulation circuitry. The FP5532 can be powered with a supply voltage from 0V to 11V and can provide an output peak current up to 1800mA, a fixed off time slow decay, a low power sleep mode, which lets the system save power when not driving the power.

Bridge Control and Decay Modes

The IN1 and IN2 input pins control the state of the OUT1 and OUT2 outputs, the IN1 and IN2 input pins control the state of the OUT1 and OUT2 outputs. Table 1 shows the logic.

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Coast/Fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/Slow decay

Table 1. H-Bridge Logic

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states: fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes, in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to one IN pin while the other is held low, to use slow decay, one IN pin is held high.

IN1	IN2	Function
PWM	0	Forward PWM/Fast decay
1	PWM	Forward PWM/Slow decay
0	PWM	Reverse PWM/Fast decay
PWM	1	Reverse PWM/Slow decay

Table 2. PWM Control of Motor Speed

Sleep Mode operation

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time, tWAKE, needs to pass before the motor driver becomes fully operational. To make the board design simple, the nSLEEP can be pulled up to the supply (VM). Recommends using a pull up resistor when this is done.

Input Under Voltage Lockout

When the FP5532 is power on, the internal circuits are held inactive until VM voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when VM is below the input UVLO threshold voltage.

Over Current Protection

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the H-bridge will be disable. The driver will be re-enabled after the OCP retry period (tOCP) has passed. If the fault condition is still present, normal operation resumes. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally.

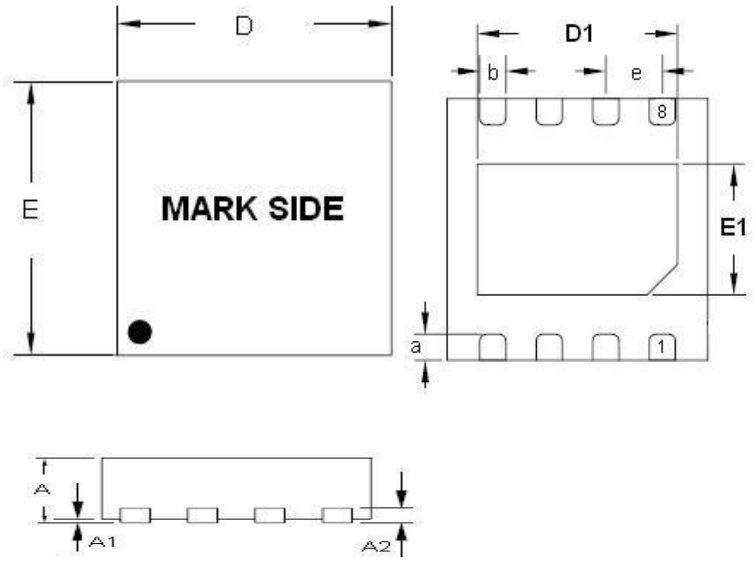
Over current conditions are detected independently on both high and low side devices. When the device occur a short to ground, supply, or across the motor winding will all result in an over current shutdown. Over current protection does not use the current sense circuitry used for PWM current control.

Over Temperature Protection

The FP5532 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, all FETs in the H-bridge will be disable. Once the die temperature has fallen to a safe level, operation will automatically resumed.

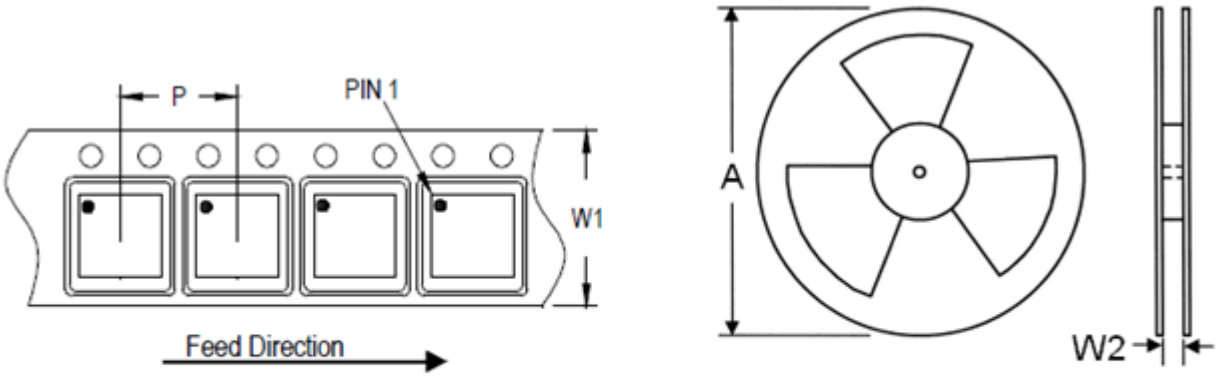
Outline Information

TDFN-8L (2mmx2mm) (pitch:0.5mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	1.90	2.10
E	1.90	2.10
a	0.20	0.40
b	0.18	0.30
e	0.45	0.55
D1	1.10	1.30
E1	0.60	0.80

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	400~1000	3,000