High Efficiency 5.5V 2A Synchronous Step Down Converter

Description

The FP6312F is a high efficiency, high frequency and pulse width modulation (PWM) synchronous DC-DC step-down converter. The 100% duty cycle feature provides low dropout operation, extending battery life in portable systems.

The internal synchronous switch increases efficiency and eliminates the need for external Schottky diode. At shutdown mode, the input supply current is less than 0.85µA. The FP6312F use the constant on time control scheme that provides fast transient response, the noise immunity and all kinds of very low ESR output capacitor for ensuring performance stabilization.

The FP6312F fault protection includes over current protection, short circuit protection, UVLO and thermal shutdown. The Internal soft-start function prevents inrush current at turn-on.

The FP6312F is offered in SOT-563-6L/SOT-23-5L/ SOT-23-6L Packages.

Features

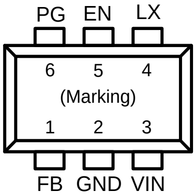
- 2.6V~5.5V Input Voltage Range
- 0.6V Reference Voltage
- 2A Output Current
- Low $R_{DS(ON)}$ for Internal Switch (Top/Bottom):
  FP6312FSDA/SDB:100/70mΩ
  FP6312FS5/S6:140/90mΩ
- Capacitor-Current-Sense Constant On Time (CCMCOT) Enables Fast Transient Response
- Pseudo 1.5MHz Switching Frequency
- Internal Soft-Start Limits the Inrush Current
- Internal Compensation Function
- 100% Duty Low Dropout Operation
- Power Good Indicator Output
- Over Current Protection
- Hiccup Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- RoHS Compliant and Halogen Free

Applications

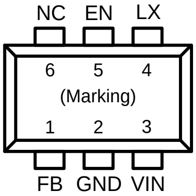
- Set Top Box
- LCD TV
- Mini-Notebook
- Net PC

Pin Assignments

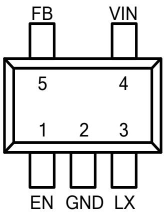
SDA Package: SOT-563-6L



SDB Package: SOT-563-6L



S5 Package: SOT-23-5L



S6 Package: SOT-23-6L

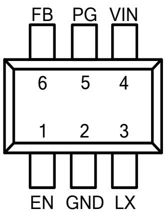


Figure 1. Pin Assignment of FP6312F

Ordering Information

FP6312F□

Package Type
SDA: SOT-563-6L
SDB: SOT-563-6L
S5: SOT-23-5L
S6: SOT-23-6L

SOT-563-6L Marking

Part Number	Product Code
FP6312FSDA	**eA**
FP6312FSDB	**eL**

SOT-23-5L Marking

Part Number	Product Code
FP6312FS5	**CS5**

SOT-23-6L Marking

Part Number	Product Code
FP6312FS6	**CS4**

Typical Application Circuit

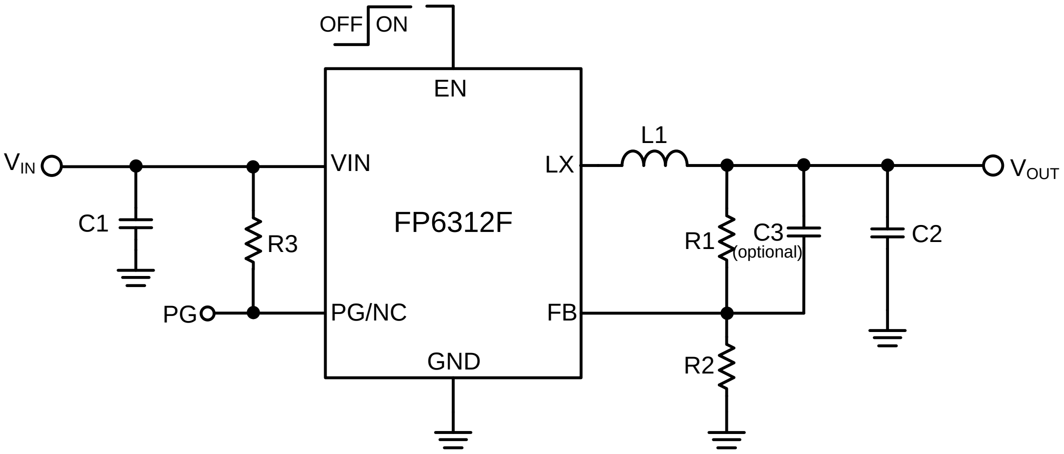


Figure 2. Schematic Diagram

VIN=5V, the recommended BOM list is as below.

V_{OUT}	C1	R1	R2	L1	C2
3.3V	22μF MLCC	453kΩ	100kΩ	2.2μH	22μF MLCC
2.5V	22μF MLCC	316kΩ	100kΩ	2.2μH	22μF MLCC
1.8V	22μF MLCC	200kΩ	100kΩ	2.2μH	22μF MLCC
1.5V	22μF MLCC	150kΩ	100kΩ	1.8μH	22μF MLCC
1.2V	22μF MLCC	100kΩ	100kΩ	1.5μH	22μF MLCC
1.0V	22μF MLCC	66.5kΩ	100kΩ	1.5μH	22μF MLCC

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No. (SOT-563-6L)	Pin No. (SOT-23-5L)	Pin No. (SOT-23-6L)	Pin Function
FB	**1**	**5**	**6**	Voltage feedback input pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.6V.
GND	**2**	**2**	**2**	Ground. pin.
VIN	**3**	**4**	**4**	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
LX	**4**	**3**	**3**	Power switching node. Connect an inductor to the drains of internal high side PMOS and low side NMOS
EN	**5**	**1**	**1**	Enable control pin. Pull high to turn the IC on, and pull low to disable the IC. Don't leave this pin floating
PG/NC	**6**	**--**	**5**	Open drain power good output pin for FP6312FSDA/FP6312FS6. No connection pin for FP6312FSDB.

Block Diagram

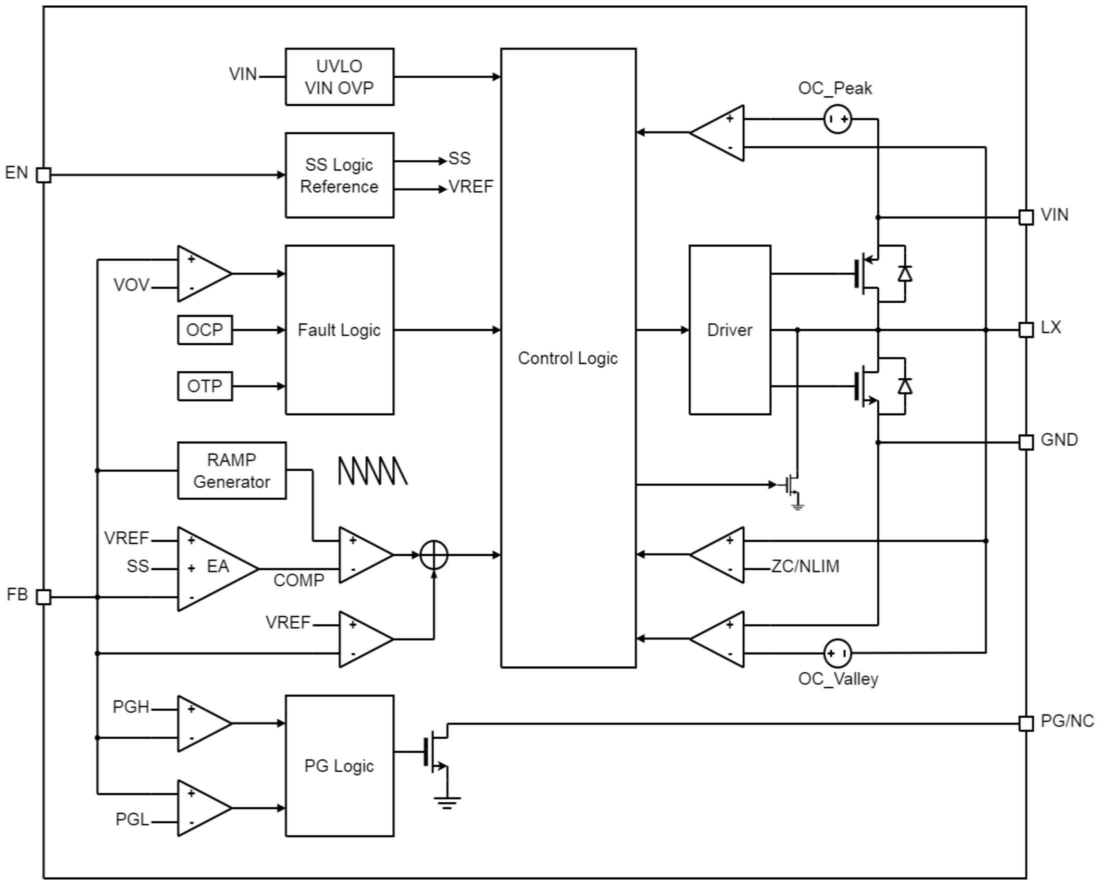


Figure 3. Block Diagram of FP6312F

Absolute Maximum Ratings (Note 1)

- VIN to GND -- -0.3V to +6.5V
- LX to GND -- -0.3V to (V_{IN} +0.3V)
- EN, FB, PG to GND -- -0.3V to V_{IN}
- Package Thermal Resistance, (θ_{JA}) (Note 2)
  - SOT-563-6L --- 103°C/W
  - SOT-23-5L --- 250°C/W
  - SOT-23-6L --- 250°C/W
- Package Thermal Resistance, (θ_{JC})
  - SOT-563-6L --- 33°C/W
  - SOT-23-5L --- 130°C/W
  - SOT-23-6L --- 110°C/W
- Maximum Junction Temperature (T_J) --- +150°C
- Lead Temperature (Soldering, 10sec.) -- +260°C
- Storage Temperature (T_S) -- -65°C to +150°C

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7. The thermal resistance greatly varies with layout, copper thickness, number of layers and PCB size.

Recommended Operating Conditions (Note 3)

- Supply Voltage (V_{IN}) -- +2.6V to +5.5V
- Junction Temperature Range -- -40°C to +125°C
- Operation Temperature Range (T_{OPR}) -- -40°C to +85°C

Note 3: The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN}=5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Supply Voltage	V_{IN}		2.6		5.5	V
V_{IN} Shutdown Supply Current	I_{SD}	EN=GND		0.1	0.85	μA
V_{IN} Quiescent Current	I_{DDQ}	V_{EN}=2, V_{FB}=1V		250		μA
Feedback Threshold Voltage	V_{FB}		0.591	0.6	0.609	V
Feedback Input Leakage Current	I_{FB}	V_{FB}=V_{IN}		0.01	1	μA
P-Channel MOSFET On-Resistance (Note 4)	$R_{DS\_ON\_P}$	FP6312FSDA/SDB		100		mΩ
		FP6312FS5/S6		140		
N-Channel MOSFET On-Resistance (Note 4)	$R_{DS\_ON\_N}$	FP6312FSDA/SDB		70		mΩ
		FP6312FS5/S6		90		
Valley Current Limit (Note 4)	I_{LIMIT}			3.4		A
Low-side Negative Current Limit (Note 4)	I_{LIMIT_L}			0.6		A
Minimum On Time	T_{ON_MIN}			60		ns
Maximum Duty Cycle	D_{MAX}				100	%
EN High-Level Input Voltage	V_{EN_H}			1	1.2	V
EN Low-Level Input Voltage	V_{EN_L}		0.4	0.8		V
Input Supply Voltage UVLO Threshold	V_{UVLO_R}	V_{IN} Rising		2.4		V
UVLO Threshold Hysteresis	V_{UVLO_HYS}			0.2		V
Internal Soft-Start Time	T_{SS}			0.8		ms
PG Rising Threshold	V_{PG_R}	V_{FB} Rising		90		%
PG Falling Threshold	V_{PG_F}	V_{FB} falling		80		%
PG Sink Current	I_{PG}	V_{PG}=0.1V		1		mA
VOUT Discharge Resistance	R_{DIS}			800		Ω
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			30		°C

Note 4: Guarantee by design.

Function Description

The FP6312F is a high efficiency step-down synchronous DC/DC converter. It has integrated high-side(FP6312FSD:100mΩ;FP6312FS5/ S6:140mΩ,typ) and low-side (FP6312FSD:70mΩ; FP6312FS5/S6:90mΩ, typ) power switches, and provides 2A continuous load current. It regulates input voltage from 2.6V to 5.5V, and down to an output voltage as low as 0.6V. The maximum operating duty cycle is 100%. Using CCMCOT control scheme provides fast transient response, which can minimize the component size without additional external compensation network.

Enable

The FP6312F EN pin provides digital control to turn on/off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator will start the soft start function. If the EN pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect EN to VIN.

Soft Start

The FP6312F employs internal soft start function to reduce input inrush current during start up. The internal soft start time will be 0.8ms.

Under Voltage Lockout

When the FP6312F is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the UVLO threshold voltage. The hysteretic of the UVLO comparator is 200mV (typ).

PG Signal Output (PG)

PG pin is an open-drain output and requires a pull up resistor. PG is actively held low in soft-start, standby and shutdown. It will be released when the output voltage rises above 90% of nominal regulation point.

Short Circuit Protection

The FP6312F provides short circuit protection function to prevent the device damage from short condition. When the short condition occurs, the oscillator frequency will be reduced naturally and hiccup mode will be triggered to prevent the inductor current increasing beyond the current limit. Once the short condition is removed, the frequency will return to normal.

Over Current Protection

The FP6312F over current protection function is implemented using cycle-by-cycle current limit architecture. The inductor current is monitored by Low-side MOSFET. When the load current increases, the inductor current also increases. When the valley inductor current reaches the current limit threshold, the output voltage starts to drop. When the over current condition is removed, the output voltage returns to the regulated value.

Over Temperature Protection

The FP6312F incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 30°C (typ).

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.6V. Thus the output voltage is:

$$V_{OUT}=0.6V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
3.3V	453kΩ	100kΩ
2.5V	316kΩ	100kΩ
1.8V	200kΩ	100kΩ
1.2V	100kΩ	100kΩ
1.0V	66.5kΩ	100kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

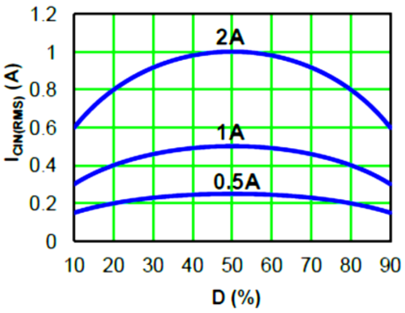
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice.

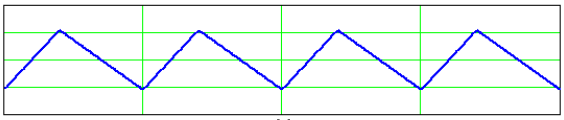
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)$$
$$+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

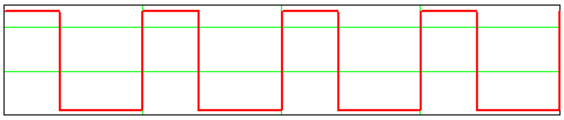
$V_{RIPPLE(ESR)}(t)$



(t)

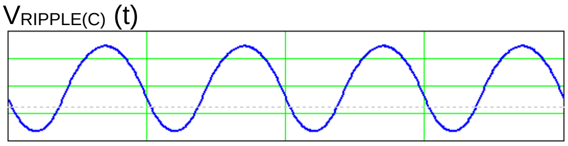
\+

$V_{RIPPLE(ESL)}(t)$



\+ (t)

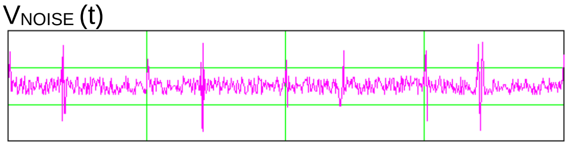
$V_{RIPPLE(C)}(t)$



(t)

\+

$V_{NOISE}(t)$



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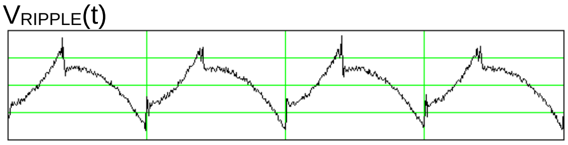
$V_{RIPPLE}(t)$



(t)

Application Information (Continued)

$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

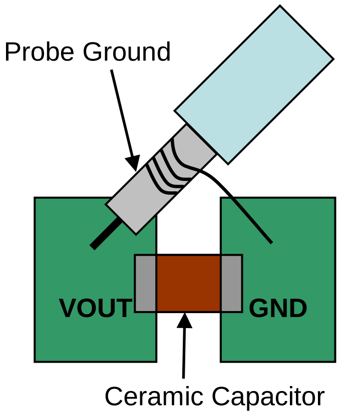
$$V_{RIPPLE(ESL)}=\frac{ESL}{L}\times V_{IN}$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC}^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

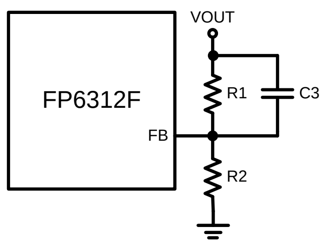
$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds IL (peak current). These are minimum requirements. To maintain control of inductor current in overload and short circuit conditions, some applications may desire current ratings up to the current limit value.

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C3 in the feedback network is recommended to improve transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C3 can be calculated with the following equation:

Application Information (Continued)

$$C3=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region.

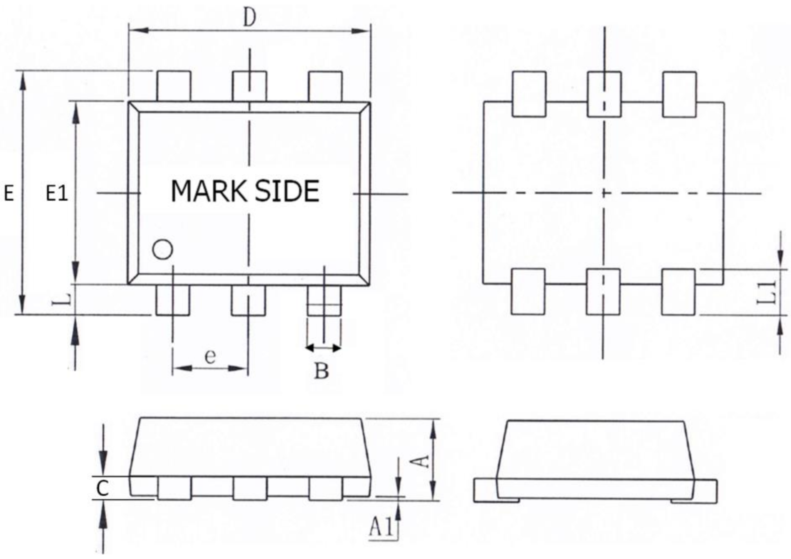
PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. Multi-layer PCB design is recommended.

Outline Information

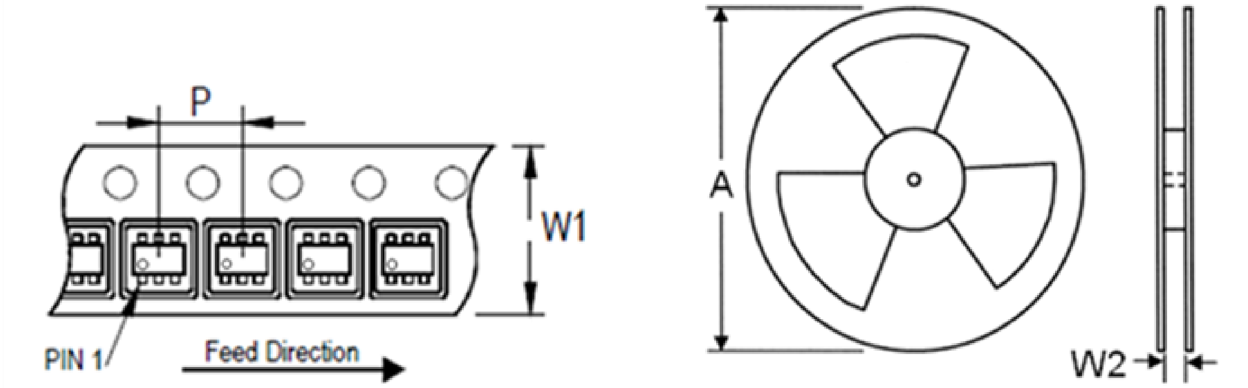
SOT-563-6L Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER MIN	DIMENSION IN MILLIMETER MAX
A	0.525	0.600
A1	0.000	0.050
B	0.170	0.270
C	0.110	0.160
D	1.500	1.700
E	1.500	1.700
E1	1.100	1.300
e	0.500 BSC	
L	0.100	0.300
L1	0.200	0.400

Note 5: Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.3mm.

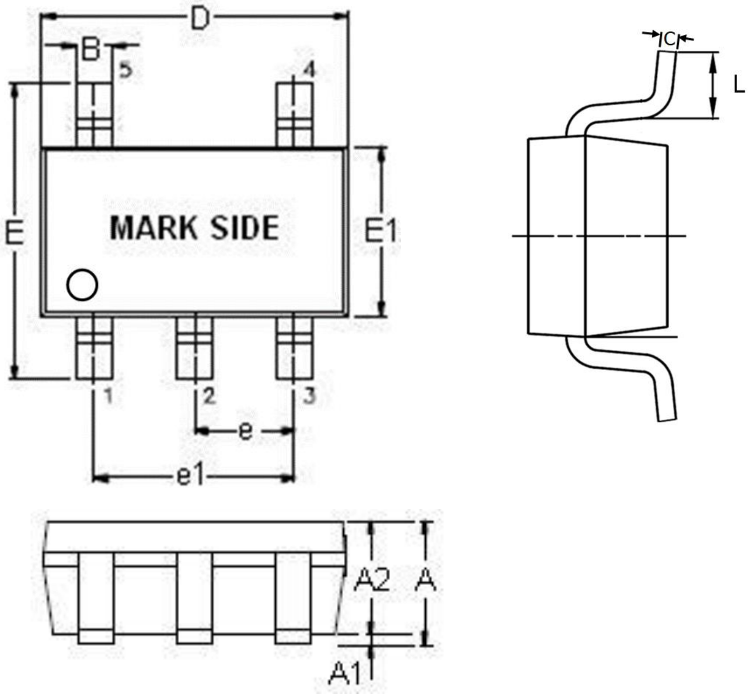
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A) in	Reel Size (A) mm	Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
8	4	7	180	8.4	300~1000	5,000

Outline Information (Continued)

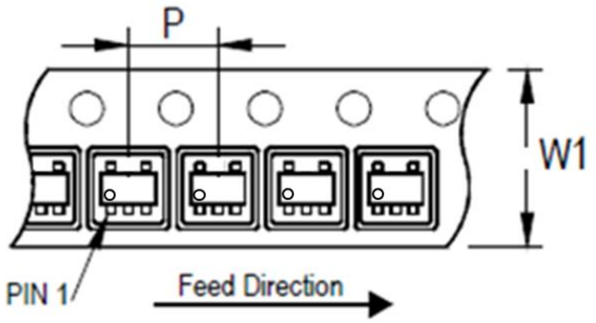
SOT-23-5L Package (Unit: mm)

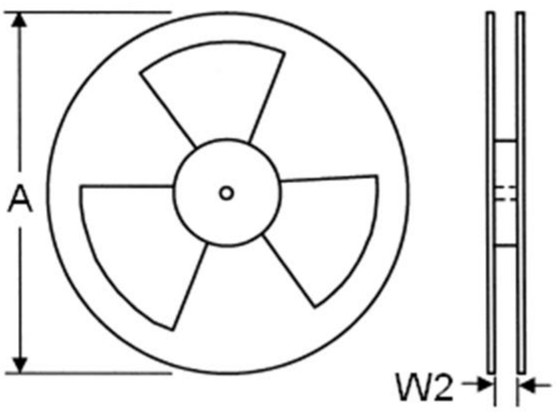


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.30
A1	0.00	0.15
A2	0.90	1.15
B	0.28	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
C	0.08	0.20
L	0.30	0.60

Note 6: Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.3mm.
Note 7: Reference JEDEC MO-178.

Carrier Dimensions

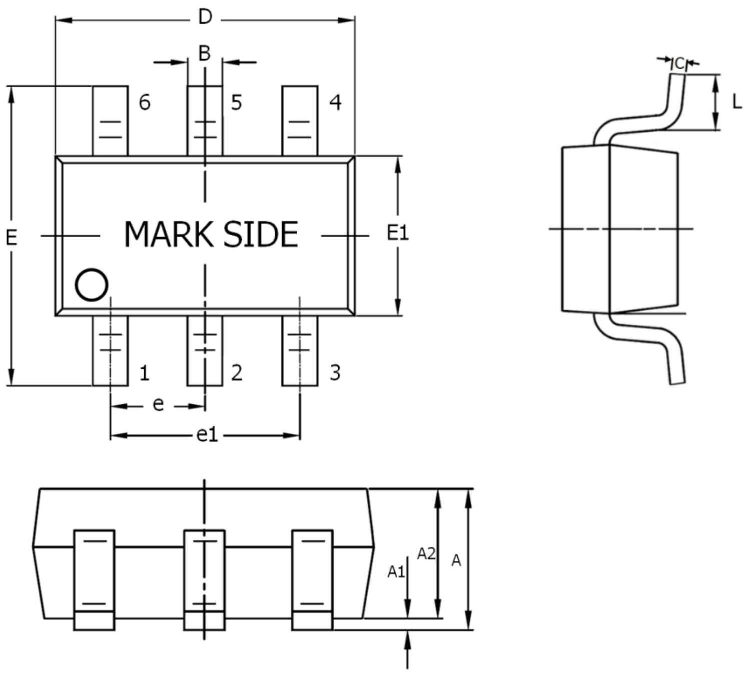




Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Outline Information (Continued)

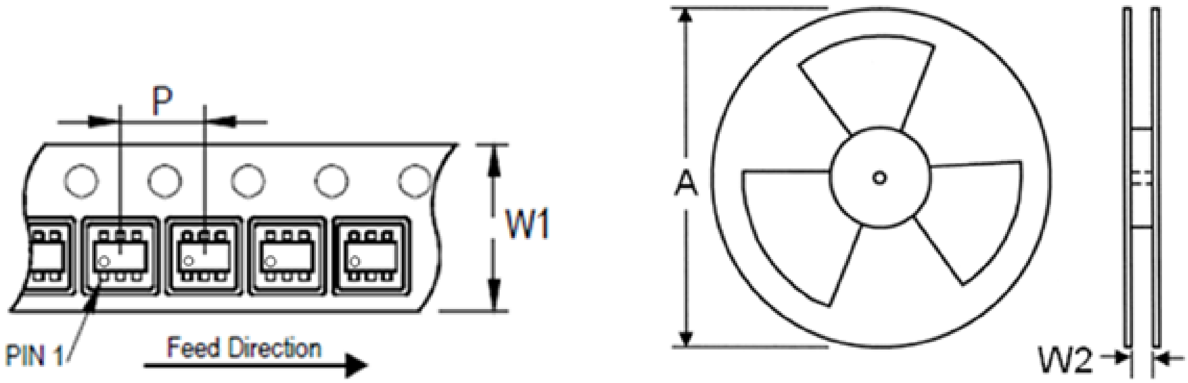
SOT-23-6L Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.30
A1	0.00	0.15
A2	0.90	1.15
B	0.28	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
C	0.08	0.20
L	0.30	0.60

Note 8: Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.3mm.
Note 9: Reference JEDEC MO-178.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.