

Integrated Multi-Channel DC-DC Converters for EPD

Description

The FP9937 is power management IC which offers a compact power solution for all voltages required by color EPD (Electro-Phoretic Display) panel. The FP9937 includes 3 negative LDOs, 3 positive LDOs, 1 negative charge pump and 1 positive charge pump to supply gate driver and source driver. A VCOM buffer is provided to bias the panel. A thermal sensor and a synchronous buck are provided for additional application. All rails are adjustable through the I2C interface to accommodate specific panel requirements.

Pin Assignments

WJ Package: TQFN-64L (7mmx7mm)

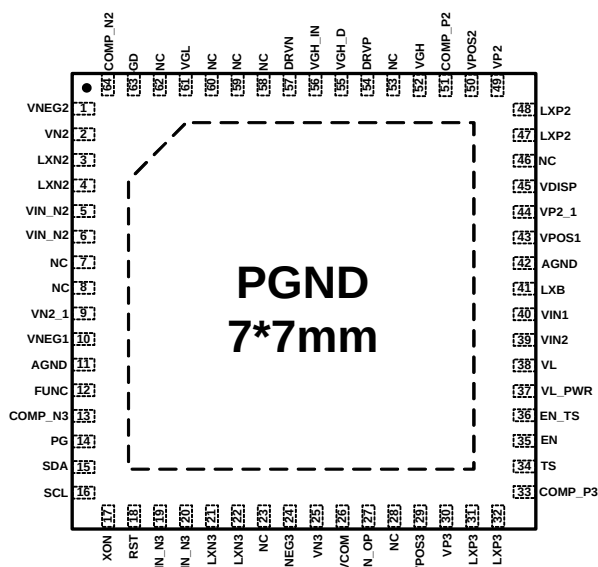


Figure 1. Pin Assignment of FP9937

Features

- 2.9V to 9.5V Input Supply Voltage, for 1 Cell Application is 2.9V to 5.5V for 2 Cells Application is 5.8V to 9.5V
- VPOS1/VNEG1: $\pm 3.5V$ to $\pm 12V$, 200mA (max.)
- VPOS2/VNEG2: $\pm 6V$ to $\pm 17V$, 300mA (max.)
- VPOS3/VNEG3: $\pm 14V$ to $\pm 27.5V$, 300mA (1Cell) /450mA (2 Cells)
- VCOM: 0V to -5V with 8-bits DAC
- VGH/ VGL: +10V to +40V/ -15V to -40V with Internal Discharge Function, 60mA(max.)
- Synchronous Buck Converter with Output Voltage Range from 1.2V to 3.3V for System Application
- Programmable Soft-Start Time
- Power Good Signal
- Protection: OCP, UVP, SCP, OTP
- Night Mode Function for Panel Off Sequence
- Thermistor Monitoring
 - ◆ -10°C to +85°C Temperature Range
 - ◆ $\pm 1^\circ C$ Accuracy from 0°C to 45°C
 - ◆ Enable/Disable by EN_TS
- I2C Slave Mode Interface (Address 3Ch)
- TQFN-64L (7mmx7mm) Package
- RoHS Compliant

Applications

- Electro-Phoretic Display (EPD) Panel
- E-Book Readers

Ordering Information

FP9937  Package Type
WJ: TQFN-64L (7mmx7mm)

Block Diagram & Typical Application Circuit

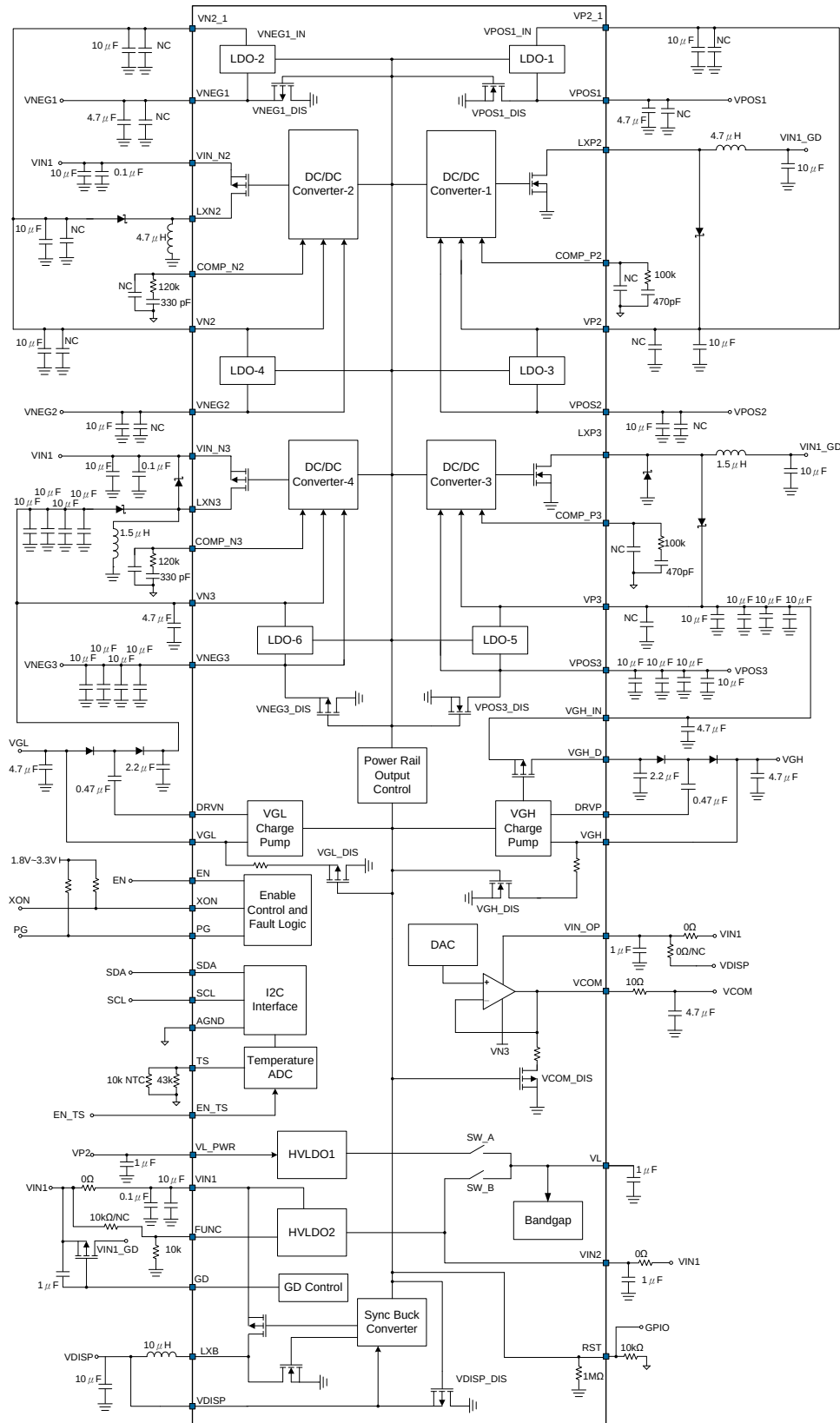


Figure2. Typical Application Circuit of FP9937 for Single Cell

Block Diagram & Typical Application Circuit (Continued)

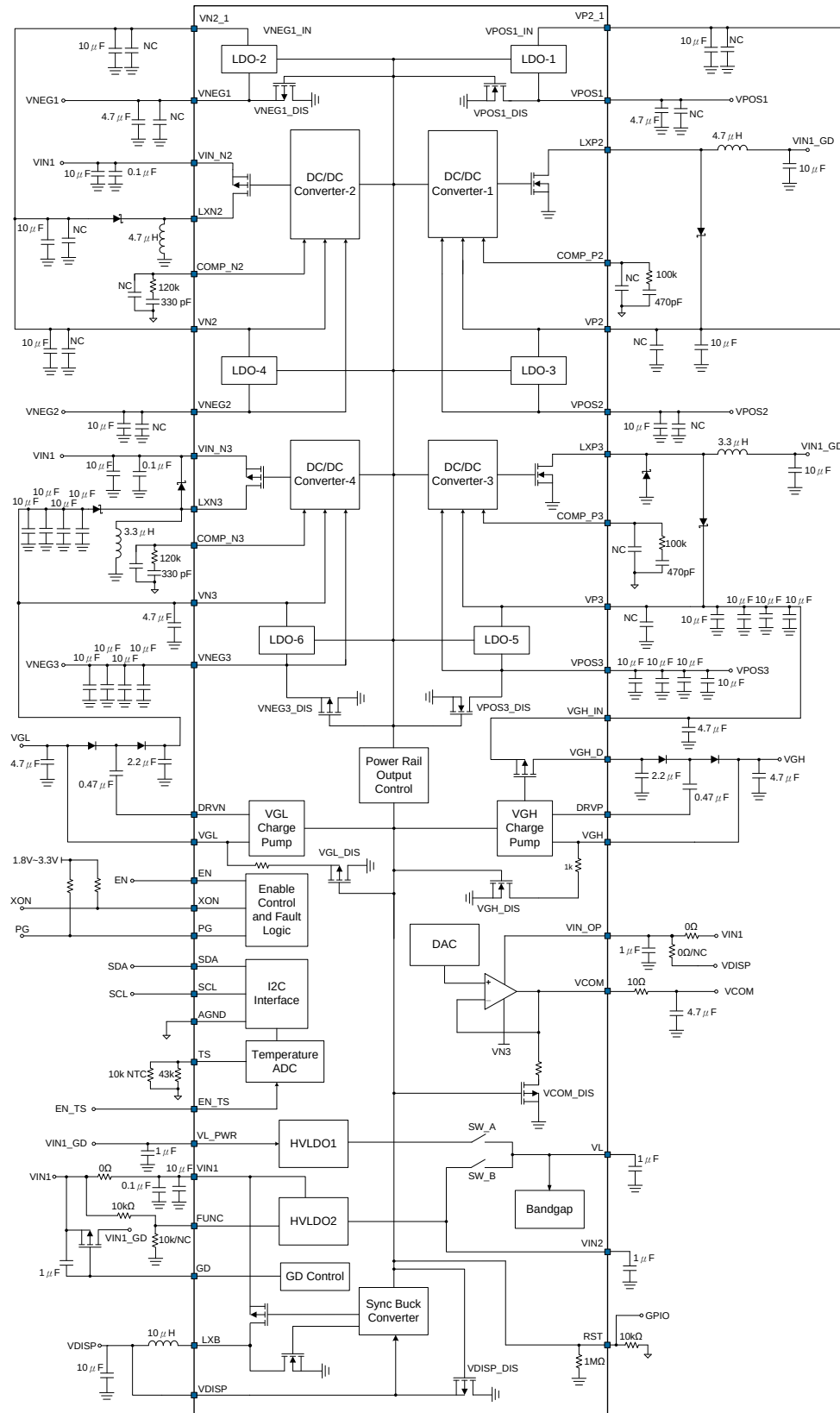


Figure3. Typical Application Circuit of FP9937 for 2 Cells

Functional Pin Description

Pin Name	Pin No	Pin I/O	Pin Function
VNEG2	1	O	VNEG2 LDO Output.
VN2	2	I	Feedback Pin for VN2 and Supply for VNEG2 Rail.
LXN2	3	I	VN2 Inductor Switch Node.
LN2	4	I	VN2 Inductor Switch Node.
VIN_N2	5	I	Input Power Supply to VN2 Rail.
VIN_N2	6	I	Input Power Supply to VN2 Rail.
NC	7	-	Not Connect.
NC	8	-	Not Connect.
VN2_1	9	I	Supply for VNEG1 Rail.
VNEG1	10	O	VNEG1 LDO Output.
AGND	11	-	Analog Ground.
FUNC	12	I	HVLDO2 enable. 1 Cell : Connect 10kΩ to GND. 2 Cell : Connect 10kΩ to VIN1.
COMP_N3	13	I	VN3 Compensation Pin.
PG	14	O	PMIC Power Good Signal for System.
SDA	15	I/O	Serial Interface (I2C) Data Input/Output.
SCL	16	I	Serial Interface (I2C) Clock Input.
XON	17	O	XON Signal for Night Mode Power-Off Sequence.
RST	18	I	Reset Pin for PMIC Register (0x00~0x19)
VIN_N3	19	I	Input Power Supply to VN3 Rail.
VIN_N3	20	I	Input Power Supply to VN3 Rail.
LXN3	21	I	VN3 Inductor Switch Node.
LN3	22	I	VN3 Inductor Switch Node.
NC	23	-	Not Connect.
VNEG3	24	O	VNEG3 LDO Output.
VN3	25	I	Feedback Pin for VN3 and Supply for VNEG3 Rail and VCOM.
VCOM	26	O	Power for Panel Common-Voltage Driver
VIN_OP	27	I	Input Power Supply to VCOM OP. Connect to VIN1 or VDISP.
NC	28	-	Not Connect.
VPOS3	29	O	VPOS3 LDO Output.
VP3	30	I	Feedback Pin for VP3 and Supply for VPOS3 Rail.

Functional Pin Description (Continued)

Pin Name	Pin No	Pin I/O	Pin Function
LXP3	31	I	VP3 Inductor Switch Node.
LXP3	32	I	VP3 Inductor Switch Node.
COMP_P3	33	I	VP3 Compensation Pin.
TS	34	I	Thermistor Input Pin.
EN	35	I	Pull this Pin High to Power Up All Output Rails.
EN_TS	36	I	Thermal Sensor Enable.
VL_PWR	37	I	HVLDO1 Input. Connect to VP2/VIN1_GD for 1 Cell/ 2 Cells.
VL	38	O	Internal LV Power.
VIN2	39	I/O	IC internal power, 1 Cells : Bandgap input. 2 Cells : HVLDO2 output.
VIN1	40	I	Input Power for Synchronous Buck Converter and UVLO Detect Point.
LXB	41	I	Synchronous Buck Converter Inductor Switch Node.
AGND	42	-	Analog Ground.
VPOS1	43	O	VPOS1 LDO Output.
VP2_1	44	I	Supply for VPOS1 Rail.
VDISP	45	I	Feedback of Synchronous Buck Converter.
NC	46	-	Not Connect.
LXP2	47	I	VP2 Inductor Switch Node.
LXP2	48	I	VP2 Inductor Switch Node.
VP2	49	I	Feedback Pin for VP2 and Supply for VPOS2 Rail.
VPOS2	50	O	VPOS2 LDO Output.
COMP_P2	51	I	VP2 Compensation Pin.
VGH	52	I	Feedback Pin for VGH.
NC	53	-	Not Connect.
DRV_P	54	O	Driver Output Pin for VGH.
VGH_D	55	O	Precharged Output for VGH.
VGH_IN	56	I	Input Power Pin for VGH_D.
DRV_N	57	O	Driver Output Pin for VGL.
NC	58	-	Not Connect.
NC	59	-	Not Connect.
NC	60	-	Not Connect.

Functional Pin Description (Continued)

Pin Name	Pin No	Pin No	Pin Function
VGL	61	I	Feedback Pin for VGL.
NC	62	-	Not Connect.
GD	63	O	Gate Driver for True Shutdown Function.
COMP_N2	64	I	VN2 Compensation Pin.
EP(PGND)	-	-	Exposed Pad. Connect Exposed Pad to Power Ground.

Power Rails Topology for Single Cell

1. VP2 & VPOS2 & VPOS1

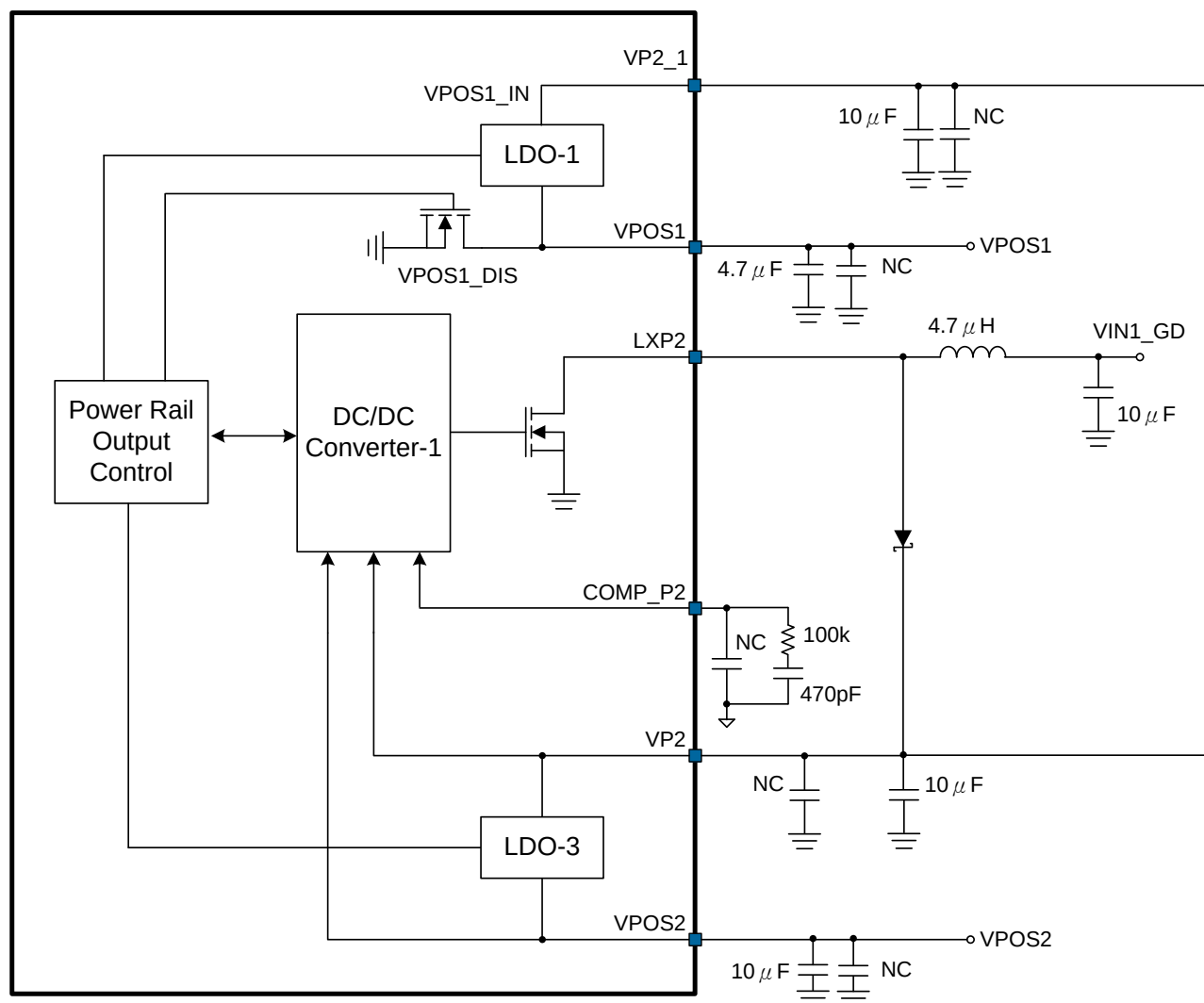


Figure 4. VP2 & VPOS2 & VPOS1 Power Rails Topology

Power Rails Topology (Continued)

2. VN2 & VNEG2 & VNEG1

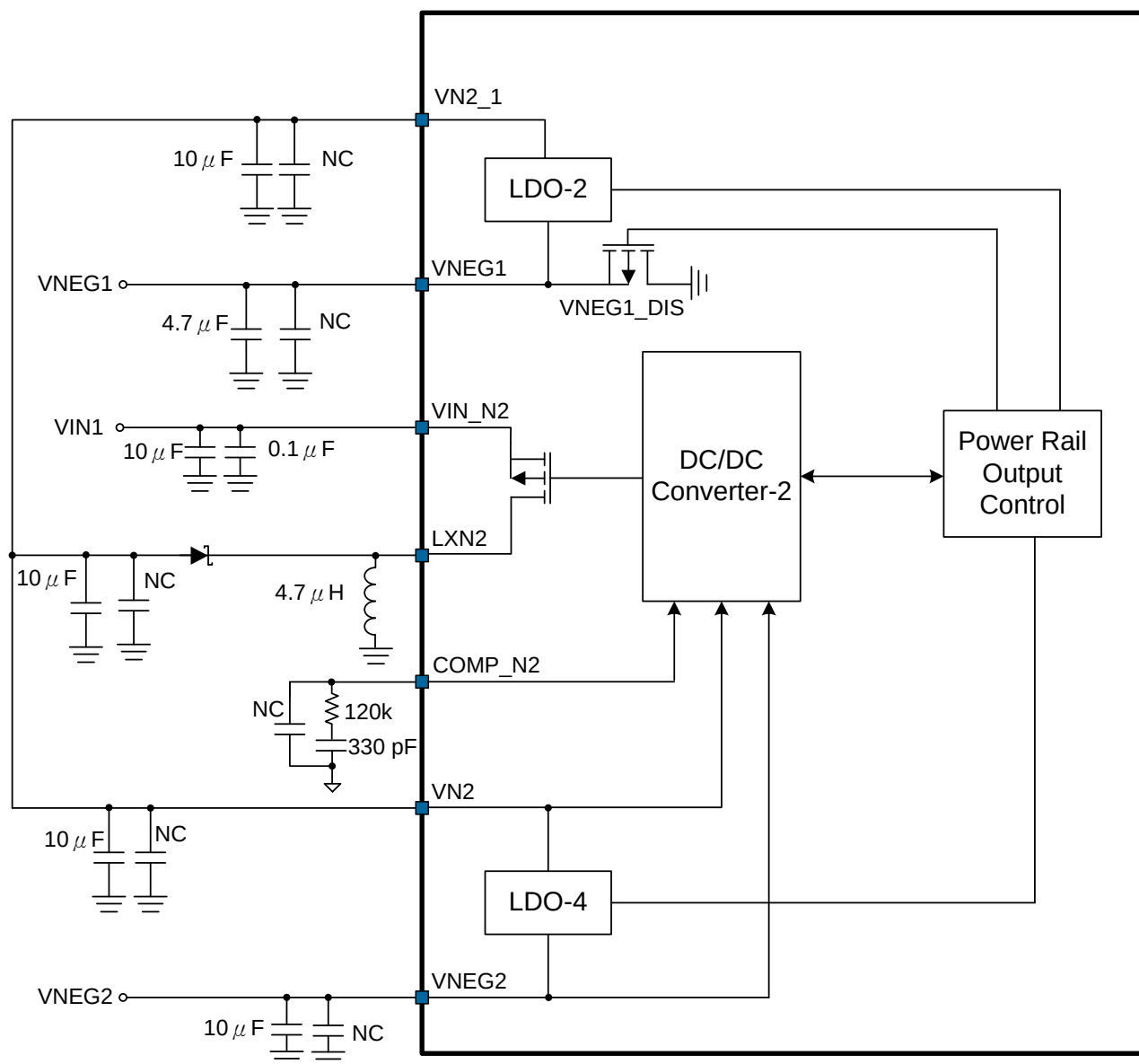


Figure 5. VN2 & VNEG2 & VNEG1 Power Rails Topology

Power Rails Topology (Continued)

3. VP3 & VPOS3 & VGH

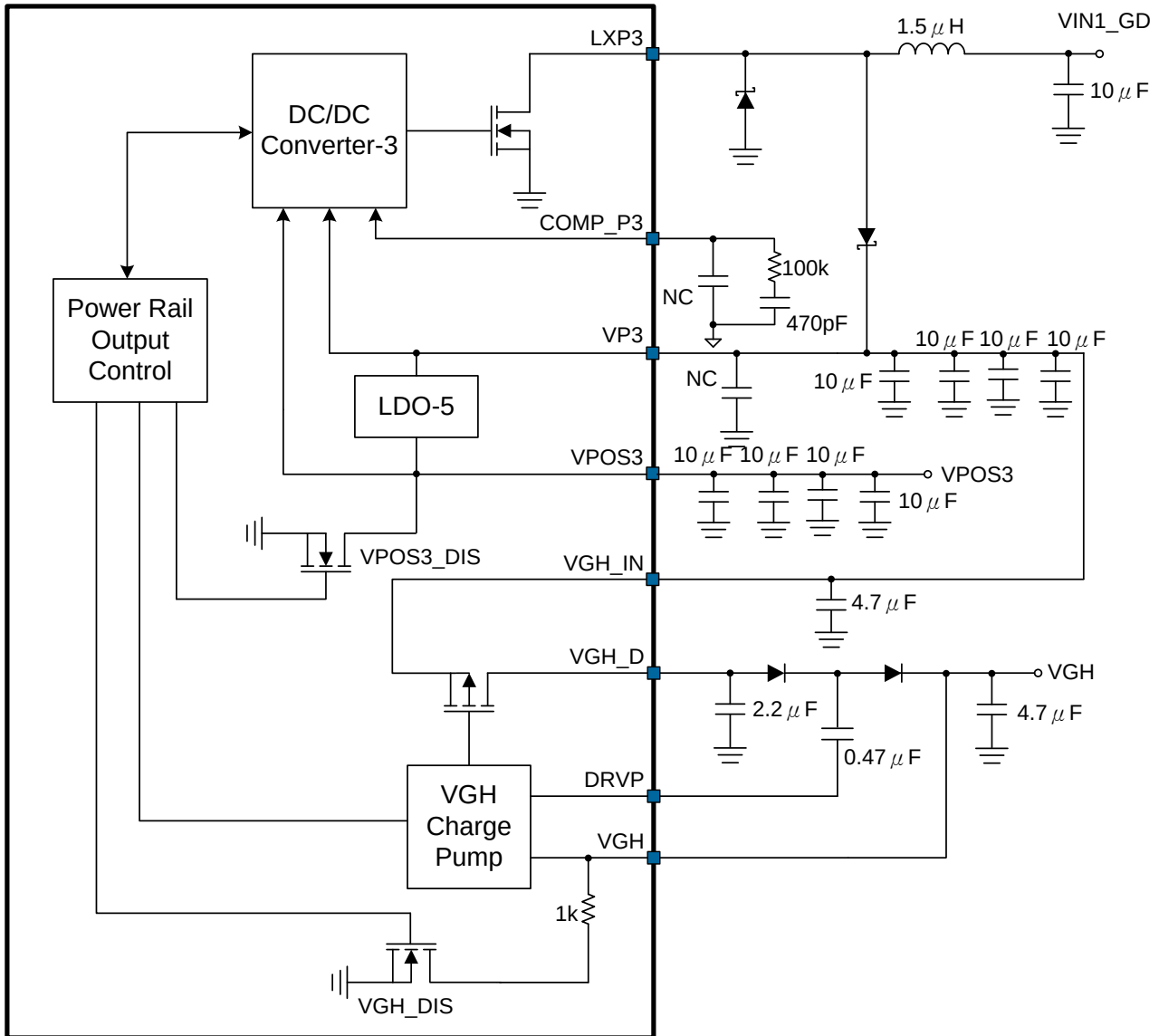


Figure 6. VP3 & VPOS3 & VGH Power Rails Topology

Power Rails Topology (Continued)

4. VN3 & VNEG3 & VGL

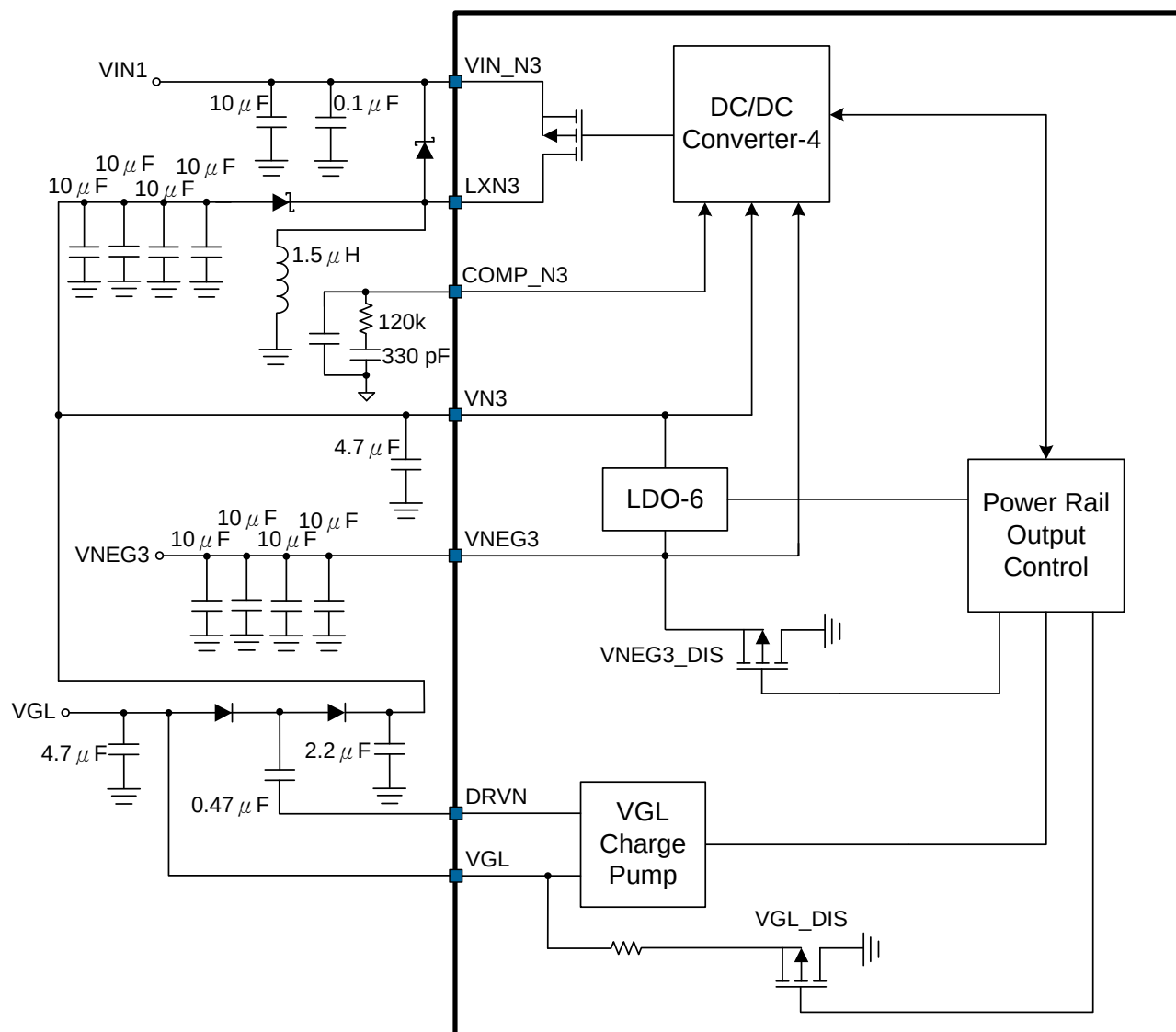


Figure 7. VN3 & VNEG3 & VGL Power Rails Topology

Power Rails Topology (Continued)

5. VCOM

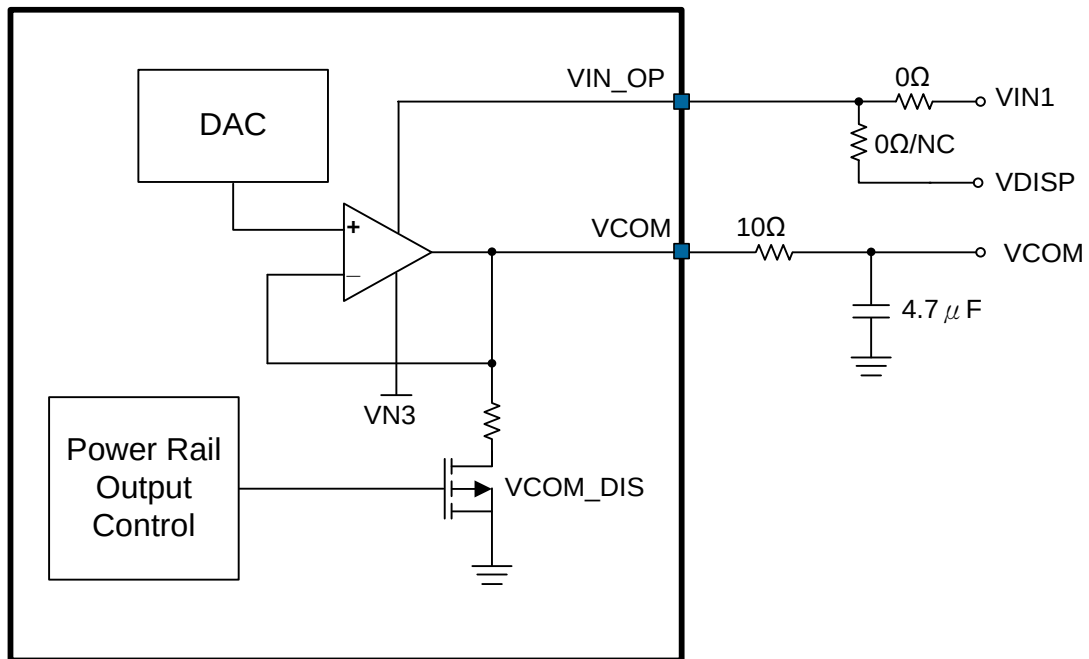


Figure 8. VCOM Power Rails Topology

Absolute Maximum Ratings (Note 1)

• VIN_N2, VIN_N3, VIN_OP, VIN1, LXB, FUNC, GD to GND	-----	-0.3V to +10V
• COMP_N3, COMP_P3, COMP_N2, COMP_P2, PG, SDA, SCL, XON, RST, TS, EN, EN_TS, VL, VIN2 to GND	-----	-0.3V to +6V
• VNEG1, VNEG2, VN2_1, VN2 to GND	-----	-19V to +0.3V
• VPOS1, VPOS2, LXP2, VL_PWR, VP2_1, VP2, VDISP to GND	-----	-0.3V to +19V
• LXN2 to GND	-----	-19V to +10V
• VN3, VNEG3, VCOM to GND	-----	-30V to +0.3V
• LXP3, VPOS3, VP3, DRVP, VGHD, VGH_IN, DRVN to GND	-----	-0.3V to +30V
• LXN3 to GND	-----	-30V to +10V
• VGL to GND	-----	-42V to +0.3V
• VGH to GND	-----	-0.3V to +42V
• Continuous Power Dissipation (T _A =+25°C)	-----	4.8W
• Package Thermal		
TQFN-64L (7mmx7mm) θ_{JA}	-----	26.03°C/W
TQFN-64L (7mmx7mm) θ_{JC}	-----	8.175°C/W
• Junction Temperature	-----	+150°C
• Storage Temperature Range	-----	-65°C to +150°C
• Lead Temperature (Soldering, 10sec)	-----	+260°C
• ESD Susceptibility		
HBM (Human Body Mode):	-----	±2KV
MM (Machine Mode):	-----	±200V
CDM(Charged-Device Mode):	-----	±500V

Note 1: Stresses beyond this listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

• Supply Voltage (VIN)	-----	+2.9V to +9.5V
• Operating Junction Temperature Range	-----	-40°C to +85°C

Electrical Characteristics

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input						
Input Voltage Range	VIN1	1S1P battery	2.9	--	5.5	V
		2S1P battery	5.8		9.5	
VIN1 UVLO Threshold (1 Cell)	VUVLO	VIN1 Rising		2.7	--	V
		Hysteresis		0.3	--	
VIN1 UVLO Threshold (2 Cells)		VIN1 Rising		5.4	--	
		Hysteresis		0.6	0.8	
VIN1 Supply Current	IIN	EN=Low, EN_TS=High	--	3	--	mA
		EN=EN_TS=High	--	4.5	--	mA
VIN1 Shutdown Current	ISD_1Cell	EN=EN_TS=Low, Input SDA, SCL=VL, VIN1=3.6V	--	--	4	uA
	ISD_2Cell	EN=EN_TS=Low, Input SDA, SCL=VL, VIN1=7.2V	--	--	8	uA
EN Input High Level	VIH_EN		1.4	--	--	V
EN Input Low Level	VIL_EN		--	--	0.4	V
EN pull-low resistor	RPL_EN			1		MΩ
EN_TS Input High Level	VIH_EN_TS		1.4	--	--	V
EN_TS Input Low Level	VIL_EN_TS		--	--	0.4	V
EN_TS pull-low resistor	RPL_EN_TS			1		MΩ
RST Input High Level	VIH_RST		1.4	--	--	V
RST Input Low Level	VIL_RST				0.4	V
RST pull-low resistor	RPL_RST			1		MΩ
Thermal Shutdown Threshold	TSD		135	150	165	°C
VP2 Boost Converter						
LXP2 Switching Frequency	FLXP2			1000		kHz
N-MOS ON-Resistance	RON_LXP2			0.15		Ω
LXP2 Current Limit	ILXP_OCP2	Sets by VP2_CL(1 A/step)	1.5	--	4.5	A
LXP2 Current Limit Accuracy	ILXP2_OCP_A		-20	--	+20	%
VP2 Soft-start Time	tSS2	Sets by SS_TIME	2	--	9	ms

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Under Voltage Protection	V _{VP2_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VP2_UVP}			40		ms
Output Short Circuit Protection	V _{VP2_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VP2_SCP}			20		us
VN2 Buck-Boost Converter						
LXN2 Switching Frequency	F _{LXN2}			1000		kHz
P-MOS ON-Resistance	R _{ON_LXN2}			0.15		Ω
LXN2 Current Limit	I _{LXN2_OCP}	Set by VN2_CL(1 A/step)	1.5	--	4.5	A
LXN2 Current Limit Accuracy	I _{LXN2_OCP_A}		-20	--	+20	%
VN2 Soft-start Time	t _{SS2}	Set by SS_TIME	2	--	9	ms
Output Under Voltage Protection	V _{VN2_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VN2_UVP}			40		ms
Output Short Circuit Protection	V _{VN2_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VN2_SCP}			20		us
VP3 Boost Converter						
LXP3 Switching Frequency	F _{LXP3}			1000		kHz
N-MOS ON-Resistance	R _{ON_LXP3}			0.1		Ω
LXP3 Current Limit	I _{LXP_OCP3}	Set by VP3_CL(1 A/step)	3	--	6	A
LXP3 Current Limit Accuracy	I _{LXP3_OCP_A}		-20	--	+20	%
VP3 Soft-start Time	t _{SS3}	Set by SS_TIME	2	--	9	ms
Output Under Voltage Protection	V _{VP3_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VP3_UVP}			40		ms
Output Short Circuit Protection	V _{VP3_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VP3_SCP}			20		us

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VN3 Buck-Boost Converter						
LXN3 Switching Frequency	F _{LXN3}			1000		kHz
P-MOS ON-Resistance	R _{ON_LXN2}			0.1		Ω
LXN3 Current Limit	I _{LXN3_OCP}	Set by VN3_CL(1 A/step)	3	--	6	A
LXN3 Current Limit Accuracy	I _{LXN3_OCP_A}		-20	--	+20	%
VN3 Soft-start Time	t _{SS3}	Set by SS_TIME	2	--	9	ms
Output Under Voltage Protection	V _{VN3_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VN3_UVP}			40		ms
Output Short Circuit Protection	V _{VN3_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VN3_SCP}			20		μs
VPOS1 LDO						
VPOS1 Output Voltage Range	V _{POS1}	01h[5:0] set Output Voltage	3.5	--	12	V
VPOS1 Output Voltage Accuracy	V _{VPOS1_A}	VPOS1=6V, I _{out} =0A	-2	--	2	%
VPOS1 Output Current	I _{POS1}	2.9V ≤ V _{in} ≤ 3.6V	--	--	150	mA
		V _{in} ≥ 3.6V	--	--	200	
VPOS1 Soft-start Time	t _{SS1}	Set by SS_TIME	2	--	5	ms
Power Good Threshold	PG_VPOS1		--	80	--	%
VPOS1 Current Limit	I _{VPOS1_OCP}			250		mA
Line Regulation		V _{IN} =2.9V~9.5V, Load=0mA	--	0.1		%/V
Load Regulation		V _{IN} =3.6V, Load=0mA~200mA	--	--	0.015	%/mA
Output Under Voltage Protection	V _{VPOS1_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VPOS1_UVP}			40		ms
Output Short Circuit Protection	V _{VPOS1_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VPOS1_SCP}			20		μs
VPOS1_DIS Open Drain N-MOS On-Resistance	R _{ON_VPOS1_DIS}		--	300	--	Ω

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VNEG1 LDO						
VNEG1 Output Voltage Range	V _{NEG1}	02h[5:0] set Output Voltage	-12	--	-3.5	V
VNEG1 Output Voltage Accuracy	V _{VNEG1_A}	VNEG1=-6V, I _{out} =0A	-2	--	2	%
VNEG1 Output Current	I _{NEG1}	2.9V ≤ V _{in} ≤ 3.6V	--	--	150	mA
		V _{in} ≥ 3.6V	--	--	200	
Power Good Threshold	PG_VNEG1		--	80	--	%
VNEG1 Soft-start Time	t _{SS1}	Set by SS_TIME	2	--	5	ms
VNEG1 Current Limit	I _{VNEG1_OCP}			250		mA
Line Regulation		V _{IN} =2.9V~9.5V, Load=0mA	--	0.1		%/V
Load Regulation		V _{IN} =3.6V, Load=0mA~200mA	--	--	0.015	%/mA
Output Under Voltage Protection	V _{VNEG1_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VNEG1_UVP}			40		ms
Output Short Circuit Protection	V _{VNEG1_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VNEG1_SCP}			20		μs
VNEG1_DIS Open Drain P-MOS On-Resistance	R _{ON_VNEG1_DIS}		--	300	--	Ω
VPOS2 LDO						
VPOS2 Output Voltage Range	V _{POS2}	03h[5:0] set Output Voltage	6	--	17	V
VPOS2 Output Voltage Accuracy	V _{VPOS2_A}	VPOS2=12V, I _{out} =0A	-2	--	2	%
VPOS2 Output Current	I _{POS2}	2.9V ≤ V _{in} ≤ 3.6V			150	mA
		V _{in} ≥ 3.6V			300	
VPOS2 Soft-start Time	t _{SS2}	Set by SS_TIME	2	--	9	ms
Power Good Threshold	PG_VPOS3			80	--	%
VPOS2 Current Limit	I _{VPOS2_OCP}			350		mA
Line Regulation		V _{IN} =2.9V~9.5V, Load=0mA	--	0.1		%/V
Load Regulation		V _{IN} =3.6V, Load=0mA~300mA	--		0.015	%/mA
Output Under Voltage Protection	V _{VPOS2_UVP}			80		%

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Under Voltage Protection Delay Time	tVPOS2_UVP			40		ms
Output Short Circuit Protection	VVPOS2_SCP			40		%
Output Short Circuit Protection Delay Time	tVPOS2_SCP			20		μs
VPOS2_DIS Open Drain N-MOS On-Resistance	R _{ON_VPOS2_DIS}		--	300	--	Ω
VNEG2 LDO						
VNEG2 Output Voltage Range	VNEG2	04h[5:0] set Output Voltage	-17	--	-6	V
VNEG2 Output Voltage Accuracy	VVNEG2_A	VNEG2=-12V, I _{out} =0A	-2	--	2	%
VNEG2 Output Current	I _{NEG2}	2.9V ≤ V _{in} < 3.6V	--	--	150	mA
		V _{in} ≥ 3.6V	--	--	300	
VNEG2 Soft-Start Time	t _{SS2}	Sets by SS_TIME	2	--	9	ms
Power Good Threshold	PG_VNEG2		--	80	--	%
VNEG2 Current Limit	I _{VNEG2_OCP}			350		mA
Line Regulation		V _{IN} =2.9V~9.5V, Load=0mA	--	0.1		%/V
Load Regulation		V _{IN} =3.6V, Load=0mA~300mA	--		0.015	%/mA
Output Under Voltage Protection	VVNEG2_UVP			80		%
Output Under Voltage Protection Delay Time	tVNEG2_UVP			40		ms
Output Short Circuit Protection	VVNEG2_SCP			40		%
Output Short Circuit Protection Delay Time	tVNEG2_SCP			20		μs
VNEG2_DIS Open Drain P-MOS On-Resistance	R _{ON_VNEG2_DIS}			300		Ω
VPOS3 LDO						
VPOS3 Output Voltage Range	VPOS3	05h[6:0] set Output Voltage	14	--	27.5	V
VPOS3 Output Voltage Accuracy	VVPOS3_A	VPOS3=24V, I _{out} =0A	-2	--	2	%
VPOS3 Output Current	I _{POS3}	2.9V ≤ V _{in} ≤ 3.6V	--	--	200	mA
		V _{in} > 3.6V, VPOS3=24V	--	--	300	
		2 Cells, VPOS3=24V			450	
VPOS3 Soft-Start Time	t _{SS3}	Sets by SS_TIME	2	--	9	ms
Power Good Threshold	PG_VPOS3			80		%

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VPOS3 Current Limit	I _{VPOS3_OCP}	1 Cell		320		mA
		2 Cells		480		
Line Regulation		VIN=2.9V~9.5V, Load=0mA	--	0.1	0.2	%/V
Load Regulation		VIN=3.6V, Load=0mA~300mA			0.015	%/mA
Output Under Voltage Protection	V _{VPOS3_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VPOS3_UVP}			40		ms
Output Short Circuit Protection	V _{VPOS3_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VPOS3_SCP}			20		μs
VPOS3_DIS Open Drain N-MOS On-Resistance	R _{ON_VPOS3_DIS}		--	300	--	Ω
VNEG3 LDO						
VNEG3 Output Voltage Range	V _{NEG3}	06h[6:0] set Output Voltage	-27.5	--	-14	V
VNEG3 Output Voltage Accuracy	V _{VNEG3_A}	VNEG3= -24V, I _{out} =0A	-2	--	2	%
VNEG3 Output Current	I _{NEG3}	2.9V≤Vin≤3.6V	--	--	200	mA
		Vin > 3.6V, VNEG3=-24V	--	--	300	
		2 Cells, VNEG3=-24V			450	
VNEG3 Soft-Start Time	t _{SS3}	Sets by SS_TIME	2	--	9	ms
Power Good Threshold	PG_VNEG3			80		%
VNEG3 Current Limit	I _{VNEG3_OCP}	1 Cell	--	320	--	mA
		2 Cells		480		
Line Regulation		VIN=2.9V~9.5V, Load=0mA	--	0.1	0.2	%/V
Load Regulation		VIN=3.6V, Load=0mA~300mA	--		0.015	%/mA
Output Under Voltage Protection	V _{VNEG3_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{VNEG3_UVP}			40		ms
Output Short Circuit Protection	V _{VNEG3_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{VNEG3_SCP}			20		μs
VNEG3_DIS Open Drain P-MOS On-Resistance	R _{ON_VNEG3_DIS}			300		Ω
Sync Buck Converter						
Input Voltage Range	VIN1		2.9		9.5	V
Frequency				750		kHz

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
soft-start time				3		ms
Output Voltage	V _{DISP}	V _{DISP} =3.3V is only used for VIN> 4.5V	1.2	1.8	3.3	V
Output Voltage Accuracy			-2		+2	%
Current limit			500		700	mA
NMOS ON-Resistance				300		mΩ
PMOS ON-Resistance				300		mΩ
Output Under Voltage Protection				80		%
Output Under Voltage Protection Delay Time				40		ms
Output Short Circuit Protection				40		%
Output Short Circuit Protection Delay Time				20		μs
Discharge Resistor				1		kΩ
VCOM Buffer						
VCOM Output Voltage Range	V _{VCOM}	09h[7:0] set Output Voltage	-5	--	0	V
VCOM Output Voltage Accuracy	V _{VCOM_A}	VCOM=-2.5V	-1.5		+1.5	%
VCOM Output Current Range	I _{VCOM}		--	--	50	mA
VCOM_DIS Open Drain N-MOS ON-Resistance	R _{ON_VCOM_DIS}			1k		Ω
Voltage difference between VIN_OP to VNEG3	V _{IN_OP} - V _{NEG3}				33	V
Positive Charge Pump (VGH)						
VGH Output Voltage Range	V _{VGH}	07h[4:0] set Output Voltage	10	--	40	V
VGH Output Voltage Accuracy	V _{VGH_A}		-3	--	+3	%
VGH Output Current Range	I _{VGH}		--	--	60	mA
DRVP Switching Frequency	F _{DRVP}			500		kHz
VGH Pre-Charge Time	t _{PC_VGH}		1		4	ms
VGH Soft-Start Time	t _{SS4_VGH}	Sets by SS_TIME	2	--	5	ms
Power Good Threshold	PG_VGH			80		%
DRVP On-Resistance High	R _{ON_DRVP_H}		--	5	--	Ω
DRVP On-Resistance LOW	R _{ON_DRVP_L}		--	3	--	Ω
VGHNM Output Voltage Range	V _{VGHNM}	15h[4:0] set Output Voltage	2	--	20	V

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VGHNM Output Voltage Accuracy	V _{VGHNM_A}		-3	--	+3	%
VGH Extension Time Range	t _{VGH_EXT}	0x14h[4:0] set Extension Time	0	--	1000	ms
VGH Extension Time Accuracy	t _{VGH_EXT_A}		-10	--	+10	%
VGHNM Extension Time Range	t _{VGHNM_EXT}	0x17h[7:0] set Extension Time	0	--	30000	ms
VGHNM Extension Time Accuracy	t _{VGHNM_EXT_A}		-10	--	+10	%
Output Under Voltage Protection	V _{GH_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{GH_UVP}			40		ms
Output Short Circuit Protection	V _{GH_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{GH_SCP}			20		μs
VGH_DIS Open Drain N-MOS On-Resistance	R _{ON_VGH_DIS1}			1		kΩ
Negative Charge Pump (VGL)						
VGL Output Voltage Range	V _{VGL}	08h[4:0] set Output Voltage	-40	--	-15	V
VGL Output Current Range	I _{VGL}			60		mA
VGH Output Voltage Accuracy	V _{GL_A}		-3	--	3	%
DRVN Switching Frequency	F _{DRVN}			500		kHz
VGL Soft-start Time	t _{SS_VGL}	Sets by SS_TIME	2		5	ms
Power Good Threshold	PG_VGL			80		%
VGL Extension Time Range	t _{VGL_EXT}	0x16h[7:0] set Extension Time	0	--	6300	ms
VGL Extension Time Accuracy	t _{VGL_EXT_A}		-10	--	+10	%
Output Under Voltage Protection	V _{GL_UVP}			80		%
Output Under Voltage Protection Delay Time	t _{GL_UVP}			40		ms
Output Short Circuit Protection	V _{GL_SCP}			40		%
Output Short Circuit Protection Delay Time	t _{GL_SCP}			20		μs
VGL_DIS Open Drain N-MOS On-Resistance	R _{ON_VGL_DIS}		--	0.6	--	kΩ
XON and Power Good Function						
XON Delay Time Range	t _{XON_DELAY}	0x19h[7:0] set Delay Time	0	--	500	ms

Electrical Characteristics (Continued)

(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XON Delay Time Accuracy	t _{XON_DELAY_A}		-10	--	+10	%
XON Len Time Range	t _{XON_LEN}		0	--	25000	ms
XON Len Time Accuracy	t _{XON_LEN_A}		-10	--	+10	%
XON Open Drain N-MOS On-Resistance	R _{ON_XON}		--	100	--	Ω
PG Open Drain N-MOS On-Resistance	R _{ON_PG}		--	100	--	Ω
VCOM Disable Delay						
Disable Delay Time	V _{COM_Tcd}		0	--	15	ms
I2C Interface						
SDA/SCL Input High Level	V _{IH_I2C}		1.4	--	--	V
SDA/SCL Input Low Level	V _{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f _{SCL}		10	--	400	kHz
Pulse Width of Suppressed Spike	T _{SP}	Deglitch time	50	--	100	ns
Data Clock High Time	t _{HIGH}		0.6			μs
Data Clock Low Time	t _{LOW}		1.3			μs
SDA/SCL Rise Time	t _r		20+0.1C _b		300	ns
SDA/SCL Fall Time	t _f		20+0.1C _b		300	ns
Hold Time (Repeated) START Condition	t _{HD:STA}		0.6			μs
Setup Time for a Repeated START Condition	t _{SU:STA}		0.6			μs
Data Hold Time	t _{HD:DAT}		0		0.9	μs
Data Setup Time (Note 2)	t _{SU:DAT}		100			ns
Setup Time for STOP Condition	t _{SU:STO}		0.6			μs
Bus Free Time Between STOP and START Condition	t _{BUF}		1.3			μs
Pulse Width of Spike Suppress	t _{SP}		0		50	ns
Capacitive Load for Each Bus Line	C _b				400	pF
Thermal Sensor						
Offset	OffsetTMS	Temperature = 25°C		1.18		V
Maximum Input Level	V _{TMS_MAX}			2.25		V

Electrical Characteristics (Continued)

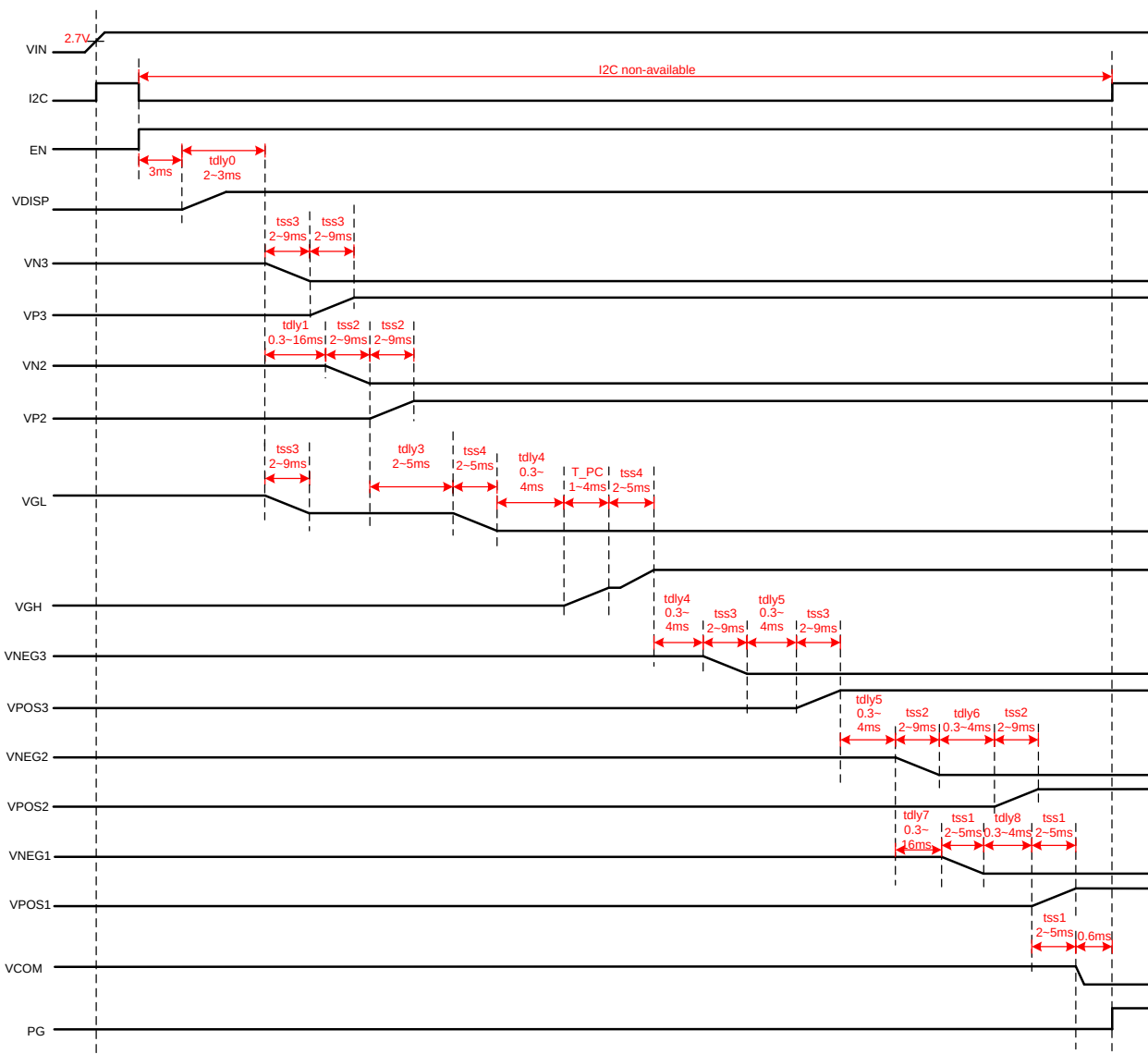
(VIN1=3.6V, typical values are at TA=25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Pull Up Resistor	R _{NTC_UP}		--	7.307	--	kΩ
External Linearization Resistor	R _{LINEAR}		--	43	--	Ω
Thermal Sensor Accuracy		0°C to 45°C	-1	--	+1	°C

Note 2: A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum t_{HD:DAT} has only to be met if the device does not stretch the Low period (t_{LOW}) of the SCL signal.

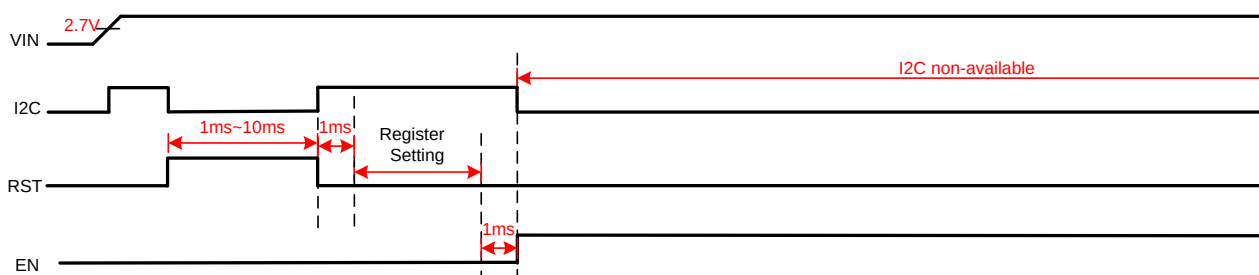
Note 3: C_b is the total capacitance of one bus line in pF, tr and tf are measured between 0.3 VDD to 0.7 VDD.

Power On Sequence



Note 4: Before activate EN, 0x10[0] must be pull high to turn on GD MOSFET.

Power On Sequence with RST

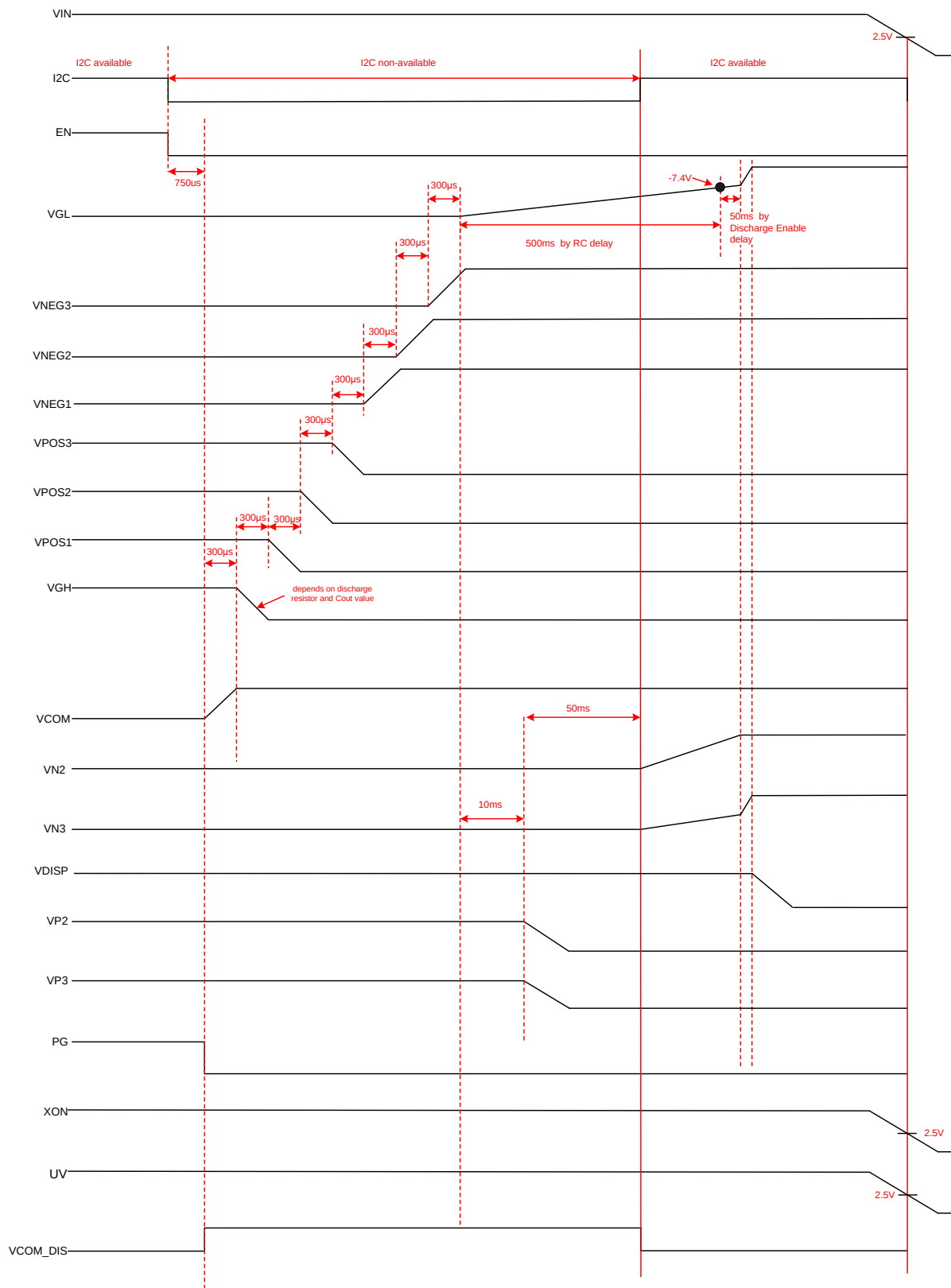


Note 5: If the RST function is not used, follow the above power on sequence without RST. In addition, power on sequence day and night mode are same.

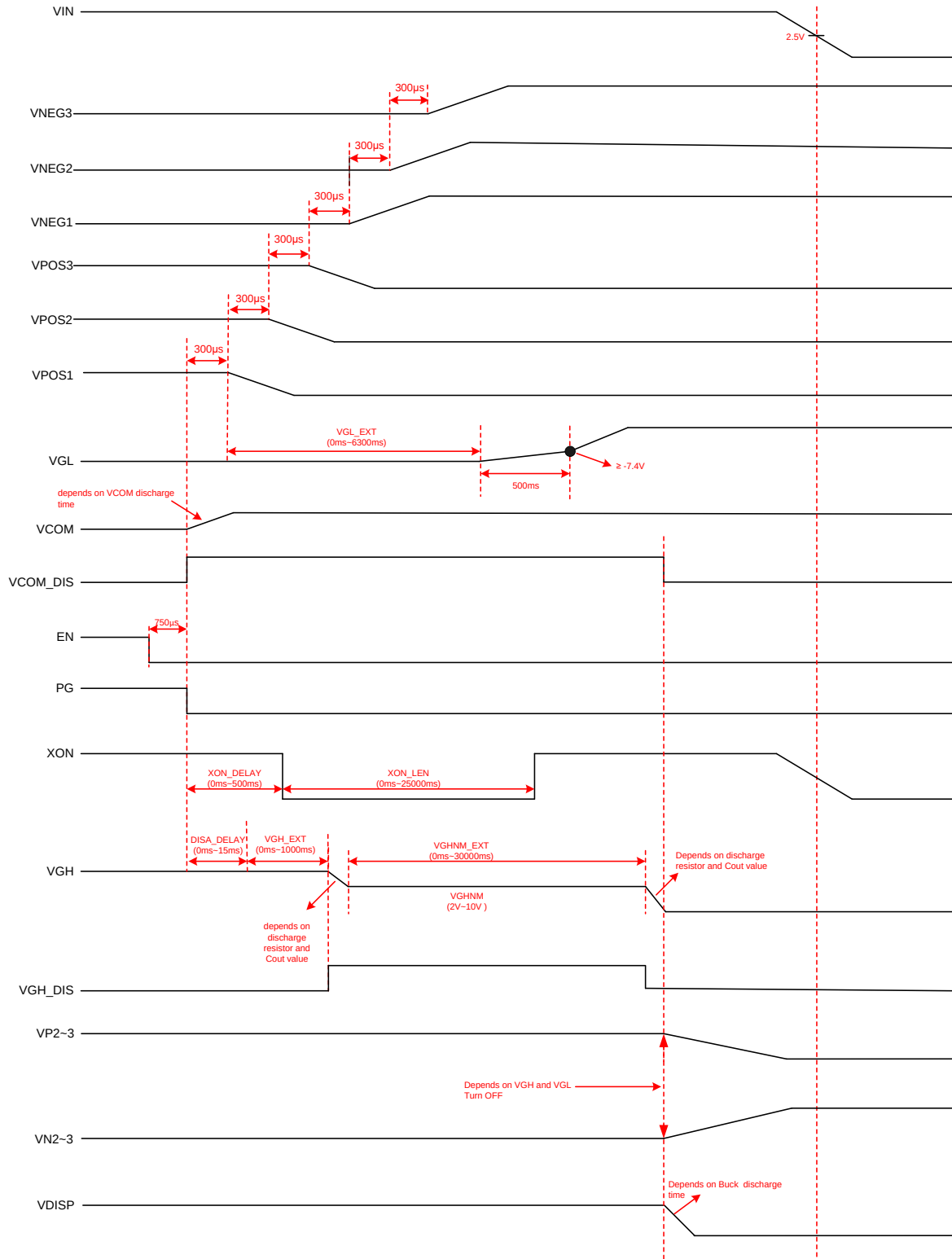
The timing diagram illustrates the power-up sequence of the AD5791R. Key events and timing parameters are as follows:

- I2C Availability:** I2C is available before EN is asserted and remains available after the power-up sequence. A period of "I2C non-available" occurs during the internal ramping of the DAC outputs.
- EN (Enable):** Asserted at the start of the power-up sequence.
- VGL (V_{GL}):** Ramps up from 0V to approximately -7.4V with a delay of $>500\text{ms}$ by RC delay. A 300 μs delay is noted between EN and VGL start.
- VNEG Signals (V_{NEG1}, V_{NEG2}, V_{NEG3}):** Ramp up sequentially, each with a 300 μs delay between steps.
- VPOS Signals (V_{POS1}, V_{POS2}, V_{POS3}):** Ramp down sequentially, each with a 300 μs delay between steps.
- VGH:** Ramps down, with a note indicating the delay "depends on discharge resistor and Cout value".
- VCOM:** Ramps up, with a 50ms delay between the completion of VGH and the start of VCOM.
- VN2 and VN3:** Ramp up, with a 10ms delay between the completion of VCOM and the start of VN2.
- VP2 and VP3:** Ramp down, with a 10ms delay between the completion of VN3 and the start of VP2.
- PG (Programmable Gain):** Asserted at the end of the power-up sequence.
- XON (X-Ray On):** Asserted after PG.
- VCOM_DIS:** Asserted at the end of the power-up sequence.

Power OFF Sequence (with VGL Discharge)



Night Mode Power OFF Sequence



Note 6: When EN to low passes 750µs(range is 680~820µs) debounce time, PMIC starts to enter the power off stage. In the power off stage, if EN suddenly becomes high, the PMIC immediately leaves the power off and enters the power on stage.

I2C Address

The IC is a slave-only device and responds to the 7-bit address 3Ch. Bit 0 is the bit of R/W function, 1 indicating read and 0 indicating write.

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	0	0	R/W

Register Address Map

Register	Address (Hex)	Name	Default CODE	Description
0	0x00	TMST_VALUE	N/A	Thermistor Value Read by ADC
1	0x01	VPOS1_SETTING	19h	Voltage Setting and Discharge EN for VPOS1. VPOS1 Default : 6V.
2	0x02	VNEG1_SETTING	19h	Voltage Setting and Discharge EN for VNEG1. VNEG1 Default : -6V.
3	0x03	VPOS2_SETTING	1Eh	Voltage Setting and Discharge EN for VPOS2. VPOS2 Default : 12V.
4	0x04	VNEG2_SETTING	1Eh	Voltage Setting and Discharge EN for VNEG2. VNEG2 Default : -12V.
5	0x05	VPOS3_SETTING	3Ch	Voltage Setting and Discharge EN for VPOS3. VPOS3 Default : 24V.
6	0x06	VNEG3_SETTING	3Ch	Voltage Setting and Discharge EN for VNEG3. VNEG3 Default : -24V.
7	0x07	VGH_SETTING	39h	Voltage Setting and Discharge EN for VGH. VGH Default : 35V. VPOS & VNEG Polarity Setting.
8	0x08	VGL_SETTING	14h	Voltage Setting for VGL. VGL Default : -35V.
9	0x09	VCOM SETTING	33h	Voltage Setting for VCOM. VCOM Default : -1V.
10	0x0A	VBK SETTING	00h	Buck Converter Setting. VBK Default : 1.2V.
11	0x0B	CURRENT_LIMIT	AAh	Current Limit Setting for VN2, VP2, VN3, VP3. VN2/VP2 CL Default : 3.5A, VN3/VP3 CL Default : 5A.
12	0x0C	SST Setting	02h	Power ON Soft Start Time Setting. Tss1/2/3 Default : 2ms/2ms/3ms.
13	0x0D	SST and Delay1 Setting	00h	Power ON Soft Start Time and Power Sequence Delay1 Setting. Tss4 Default : 2ms. TDLY1 Default : 0.3ms.
14	0x0E	Delay3~6 Setting	00h	Power Sequence Delay3~6 Setting. TDLY3/4/5/6 Default : 2ms/0.3ms/0.3ms/0.3ms.
15	0x0F	Delay7、8 Setting	00h	Power Sequence Delay7、8 Setting and Discharge EN for VGL. TDLY7/8 Default : 0.3ms/0.3ms.
16	0x10	Gate Driver Control (GD)	00h	Gate Driver Control for True Shutdown
17	0x11	Digital_ENTS	00h	Update TMST_VALUE with This Register.
18	0x12	Function Control	00h	Function Control
19	0x13	Disable Delay Setting	00h	Disable Delay (Night mode)
20	0x14	VGH_EXT Setting	00h	VGH Extension Time Setting (Night mode)
21	0x15	VGHNM_Setting	00h	Voltage Setting for VGHNM (Night mode)

Register Address Map (Continued)

Register	Address (Hex)	Name	Default Value	Description
22	0x16	VGL_EXT	00h	VGL Extension Time Setting (Night mode)
23	0x17	VGHNM_EXT	00h	VGHNM Len Time Setting (Night mode)
24	0x18	XON_DELAY	00h	XON Delay Time Setting (Night mode)
25	0x19	XON_LEN	00h	XON Len Time Setting (Night mode)
26	0x1A	Fault Flag 1	00h	Fault Flag with Protection
27	0x1B	Fault Flag 2	00h	Fault Flag with Protection

THERMISTOR READOUT (TMST_VALUE)

Address – 0x00h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TMST_VALUE [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	NA	NA	NA	NA	NA	NA	NA	NA

TMST_VALUE	Temperature	TMST_VOLTAGE	TMST_VALUE	Temperature	TMST_VOLTAGE
80H~F5H	< -10°C	<1.6911V	00h	0°C	1.5766V
F6h	-10°C	1.6911V	01h	1°C	1.5626V
F7h	-9°C	1.6808V	02h	2°C	1.5498V
F8h	-8°C	1.6705V	03h	3°C	1.5369V
F9h	-7°C	1.6596V	04h	4°C	1.5231V
Fah	-6°C	1.6484V	05h	5°C	1.5093V
FBh	-5°C	1.648V	06h	6°C	1.4943V
FCh	-4°C	1.625V	07h	7°C	1.4804V
FDh	-3°C	1.6138V	08h	8°C	1.4646V
FEh	-2°C	1.6019V	09h	9°C	1.4499V
FFh	-1°C	1.5888V	0Ah	10°C	1.4339V
			0Bh	11°C	1.4191V
			0Ch	12°C	1.4034V
			0Dh	13°C	1.3875V
			0Eh	14°C	1.3709V
			0Fh	15°C	1.3551V
			10h	16°C	1.3382V
			11h	17°C	1.3222V
			12h	18°C	1.3046V
			13h	19°C	1.2878V

TMST_VALUE	Temperature	TMST_VOLTAGE	TMST_VALUE	Temperature	TMST_VOLTAGE
14h	20°C	1.2710V	39h	57°C	0.6693V
15h	21°C	1.2542V	3Ah	58°C	0.6563V
16h	22°C	1.2363 V	3Bh	59°C	0.6426V
17h	23°C	1.2195 V	3Ch	60°C	0.6295V
18h	24°C	1.2030 V	3Dh	61°C	0.6173V
19h	25°C	1.1843 V	3Eh	62°C	0.6042V
1Ah	26°C	1.1676 V	3Fh	63°C	0.5932V
1Bh	27°C	1.1507 V	40h	64°C	0.5813V
1Ch	28°C	1.1323 V	41h	65°C	0.5694V
1Dh	29°C	1.1157 V	42h	66°C	0.5574V
1Eh	30°C	1.098 V	43h	67°C	0.5451V
1Fh	31°C	1.0802 V	44h	68°C	0.5341V
20h	32°C	1.0636 V	45h	69°C	0.5227V
21h	33°C	1.0471 V	46h	70°C	0.5118V
22h	34°C	1.0286 V	47h	71°C	0.5017V
23h	35°C	1.0118 V	48h	72°C	0.4914V
24h	36°C	0.995 V	49h	73°C	0.4811V
25H	37°C	0.9784V	4Ah	74°C	0.4709V
26h	38°C	0.9617 V	4Bh	75°C	0.4615V
27h	39°C	0.945V	4Ch	76°C	0.4514V
28h	40°C	0.9283V	4Dh	77°C	0.4421V
29h	41°C	0.9124V	4Eh	78°C	0.4318V
2Ah	42°C	0.8948V	4Fh	79°C	0.4235V
2Bh	43°C	0.8791V	50h	80°C	0.4143V
2Ch	44°C	0.8631V	51h	81°C	0.4059V
2Dh	45°C	0.8474V	52h	82°C	0.3975V
2Eh	46°C	0.8313V	53h	83°C	0.3889V
2Fh	47°C	0.8157V	54h	84°C	0.3815V
30h	48°C	0.7998V	55h	85°C	0.3732V
31h	49°C	0.7847V			
32h	50°C	0.7697V			
33h	51°C	0.7548V			
34h	52°C	0.7399V			
35h	53°C	0.7262V			
36h	54°C	0.712V			
37h	55°C	0.6972V			
38h	56°C	0.6835V			

VPOS1 Output Voltage (VPOS1_SETTING)

Address – 0x01h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS1_DISC	DON'T Reserve	VPOS1_LVL [5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	NA	0	1	1	0	0	1

Name	Description
VPOS1_DISC	Discharge EN Control for VPOS1 0: Disable; 1: Enable Default: 0
VPOS1_LVL [5:0]	Voltage setting for VPOS1 3.5V~12V; 100mV/Step from 3.5V to 8.8V, 200mV/Step from 8.8V to 10V, 500mV/Step from 10V to 12V. Default: 0x19

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	3.5V	16h	5.7V	2Ch	7.9V
01h	3.6V	17h	5.8V	2Dh	8V
02h	3.7V	18h	5.9V	2Eh	8.1V
03h	3.8V	19h	6V	2Fh	8.2V
04h	3.9V	1Ah	6.1V	30h	8.3V
05h	4 V	1Bh	6.2V	31h	8.4V
06h	4.1V	1Ch	6.3V	32h	8.5V
07h	4.2V	1Dh	6.4V	33h	8.6V
08h	4.3V	1Eh	6.5V	34h	8.7V
09h	4.4V	1Fh	6.6V	35h	8.8V
0Ah	4.5V	20h	6.7V	36h	9V
0Bh	4.6V	21h	6.8V	37h	9.2V
0Ch	4.7V	22h	6.9V	38h	9.4V
0Dh	4.8V	23h	7V	39h	9.6V
0Eh	4.9V	24h	7.1V	3Ah	9.8V
0Fh	5V	25h	7.2V	3Bh	10V
10h	5.1V	26h	7.3V	3Ch	10.5V
11h	5.2V	27h	7.4V	3Dh	11V
12h	5.3V	28h	7.5V	3Eh	11.5V
13h	5.4V	29h	7.6V	3Fh	12V
14h	5.5V	2Ah	7.7V		
15h	5.6V	2Bh	7.8V		

VNEG1 Output Voltage (VNEG1_SETTING)

Address – 0x02h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG1_DISC	DON'T Reserve	VNEG1_LVL [5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	NA	0	1	1	0	0	1

Name	Description
VNEG1_DISC	Discharge EN Control for VNEG1 0: Disable; 1: Enable Default: 0
VNEG1_LVL [5:0]	Voltage setting for VNEG1 -3.5V~-12V; 100mV/Step from -3.5V to -8.8V, 200mV/Step from -8.8V to -10V, 500mV/Step from -10V to -12V. Default: 0x19

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	-3.5V	16h	-5.7V	2Ch	-7.9V
01h	-3.6V	17h	-5.8V	2Dh	-8V
02h	-3.7V	18h	-5.9V	2Eh	-8.1V
03h	-3.8V	19h	-6V	2Fh	-8.2V
04h	-3.9V	1Ah	-6.1V	30h	-8.3V
05h	-4V	1Bh	-6.2V	31h	-8.4V
06h	-4.1V	1Ch	-6.3V	32h	-8.5V
07h	-4.2V	1Dh	-6.4V	33h	-8.6V
08h	-4.3V	1Eh	-6.5V	34h	-8.7V
09h	-4.4V	1Fh	-6.6V	35h	-8.8V
0Ah	-4.5V	20h	-6.7V	36h	-9V
0Bh	-4.6V	21h	-6.8V	37h	-9.2V
0Ch	-4.7V	22h	-6.9V	38h	-9.4V
0Dh	-4.8V	23h	-7V	39h	-9.6V
0Eh	-4.9V	24h	-7.1V	3Ah	-9.8V
0Fh	-5V	25h	-7.2V	3Bh	-10V
10h	-5.1V	26h	-7.3V	3Ch	-10.5V
11h	-5.2V	27h	-7.4V	3Dh	-11V
12h	-5.3V	28h	-7.5V	3Eh	-11.5V
13h	-5.4V	29h	-7.6V	3Fh	-12V
14h	-5.5V	2Ah	-7.7V		
15h	-5.6V	2Bh	-7.8V		

VPOS2 Output Voltage (VPOS2_SETTING)

Address – 0x03h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS2_DISC	DON'T Reserve	VPOS2_LVL [5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	NA	0	1	1	1	1	0

Name	Description
VPOS2_DISC	Discharge EN Control for VPOS2 0: Disable; 1: Enable Default: 0
VPOS2_LVL [5:0]	Voltage setting for VPOS2 6V~15V; 200mV/Step Default: 0x1E

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	6V	16h	10.4V	2Ch	14.8V
01h	6.2V	17h	10.6V	2Dh	15V
02h	6.4V	18h	10.8V		
03h	6.6V	19h	11V		
04h	6.8V	1Ah	11.2V		
05h	7V	1Bh	11.4V		
06h	7.2V	1Ch	11.6V		
07h	7.4V	1Dh	11.8V		
08h	7.6V	1Eh	12V		
09h	7.8V	1Fh	12.2V		
0Ah	8V	20h	12.4V		
0Bh	8.2V	21h	12.6V		
0Ch	8.4V	22h	12.8V		
0Dh	8.6V	23h	13V		
0Eh	8.8V	24h	13.2V		
0Fh	9V	25h	13.4V		
10h	9.2V	26h	13.6V		
11h	9.4V	27h	13.8V		
12h	9.6V	28h	14V		
13h	9.8V	29h	14.2V		
14h	10V	2Ah	14.4V		
15h	10.2V	2Bh	14.6V		

VNEG2 Output Voltage (VNEG2_SETTING)

Address – 0x04h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG2_DISC	DON'T Reserve	VNEG2_LVL [5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	NA	0	1	1	1	1	0

Name	Description
VNEG2_DISC	Discharge EN Control for VNEG2 0: Disable; 1: Enable Default: 0
VNEG2_LVL [5:0]	Voltage setting for VNEG2 -6V~-15V; 200mV/Step Default: 0x1E

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	-6V	16h	-10.4V	2Ch	-14.8V
01h	-6.2V	17h	-10.6V	2Dh	-15V
02h	-6.4V	18h	-10.8V		
03h	-6.6V	19h	-11V		
04h	-6.8V	1Ah	-11.2V		
05h	-7V	1Bh	-11.4V		
06h	-7.2V	1Ch	-11.6V		
07h	-7.4V	1Dh	-11.8V		
08h	-7.6V	1Eh	-12V		
09h	-7.8V	1Fh	-12.2V		
0Ah	-8V	20h	-12.4V		
0Bh	-8.2V	21h	-12.6V		
0Ch	-8.4V	22h	-12.8V		
0Dh	-8.6V	23h	-13V		
0Eh	-8.8V	24h	-13.2V		
0Fh	-9V	25h	-13.4V		
10h	-9.2V	26h	-13.6V		
11h	-9.4V	27h	-13.8V		
12h	-9.6V	28h	-14V		
13h	-9.8V	29h	-14.2V		
14h	-10V	2Ah	-14.4V		
15h	-10.2V	2Bh	-14.6V		

VPOS3 Output Voltage (VPOS3_SETTING)

Address – 0x05h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VPOS3_DISC	VPOS3_LVL [6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	0	0

Name	Description
VPOS3_DISC	Discharge EN Control for VPOS3 0: Disable; 1: Enable Default: 0
VPOS3_LVL [6:0]	Voltage setting for VPOS3 14V~27.5V; 250mV/Step, VPOS3>VPOS2, VPOS3>VPOS1 Default: 0x3C

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	14V	16h	14.5V	2Ch	20V
01h	14V	17h	14.75V	2Dh	20.25V
02h	14V	18h	15V	2Eh	20.5V
03h	14V	19h	15.25V	2Fh	20.75V
04h	14V	1Ah	15.5V	30h	21V
05h	14V	1Bh	15.75V	31h	21.25V
06h	14V	1Ch	16V	32h	21.5V
07h	14V	1Dh	16.25V	33h	21.75V
08h	14V	1Eh	16.5V	34h	22V
09h	14V	1Fh	16.75V	35h	22.25V
0Ah	14V	20h	17V	36h	22.5V
0Bh	14V	21h	17.25V	37h	22.75V
0Ch	14V	22h	17.5V	38h	23V
0Dh	14V	23h	17.75V	39h	23.25V
0Eh	14V	24h	18V	3Ah	23.5V
0Fh	14V	25h	18.25V	3Bh	23.75V
10h	14V	26h	18.5V	3Ch	24V
11h	14V	27h	18.75V		
12h	14V	28h	19V		
13h	14V	29h	19.25V		
14h	14V	2Ah	19.5V	49h	27.25V
15h	14.25V	2Bh	19.75V	4Ah	27.5V

VNEG3 Output Voltage (VNEG3_SETTING)

Address – 0x06h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VNEG3_DISC	VNEG3_LVL [6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	0	0

Name	Description
VNEG3_DISC	Discharge EN Control for VNEG3 0: Disable; 1: Enable Default: 0
VNEG3_LVL [6:0]	Voltage setting for VNEG3 -14V~27.5V; 250mV/Step, VNEG3<VNEG2, VNEG3<VNEG1 Default: 0x3C

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	-14V	16h	-14.5V	2Ch	-20V
01h	-14V	17h	-14.75V	2Dh	-20.25V
02h	-14V	18h	-15V	2Eh	-20.5V
03h	-14V	19h	-15.25V	2Fh	-20.75V
04h	-14V	1Ah	-15.5V	30h	-21V
05h	-14V	1Bh	-15.75V	31h	-21.25V
06h	-14V	1Ch	-16V	32h	-21.5V
07h	-14V	1Dh	-16.25V	33h	-21.75V
08h	-14V	1Eh	-16.5V	34h	-22V
09h	-14V	1Fh	-16.75V	35h	-22.25V
0Ah	-14V	20h	-17V	36h	-22.5V
0Bh	-14V	21h	-17.25V	37h	-22.75V
0Ch	-14V	22h	-17.5V	38h	-23V
0Dh	-14V	23h	-17.75V	39h	-23.25V
0Eh	-14V	24h	-18V	3Ah	-23.5V
0Fh	-14V	25h	-18.25V	3Bh	-23.75V
10h	-14V	26h	-18.5V	3Ch	-24V
11h	-14V	27h	-18.75V		
12h	-14V	28h	-19V		
13h	-14V	29h	-19.25V		
14h	-14V	2Ah	-19.5V	49h	-27.25V
15h	-14.25V	2Bh	-19.75V	4Ah	-27.5V

VGH Output Voltage (VGH_SETTING)

Address – 0x07h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGH_DISC	VPOS POL	VNEG POL	VGH_LVL [4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	0	0	1

Name	Description
VGH_DISC	Discharge EN Control for VGH Discharge Function 0: Disable; 1: Enable Default: 0
VPOS POL	VPOS1/2 polarity setting 0: VPOS1<VPOS2; 1: VPOS1>VPOS2 Default: 0
VNEG POL	VNEG1/2 polarity setting 0: VNEG1<VNEG2; 1: VNEG1>VNEG2 Default: 1
VGH_LVL [4:0]	Voltage setting for VGH 10V~40V; 1V/Step Default: 0x19

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	10V	0Bh	21V	16h	32V
01h	11V	0Ch	22V	17h	33V
02h	12V	0Dh	23V	18h	34V
03h	13V	0Eh	24V	19h	35V
04h	14V	0Fh	25V	1Ah	36V
05h	15V	10h	26V	1Bh	37V
06h	16V	11h	27V	1Ch	38V
07h	17V	12h	28V	1Dh	39V
08h	18V	13h	29V	1Eh	40V
09h	19V	14h	30V		
0Ah	20V	15h	31V		

VGL Output Voltage
Address – 0x08h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve			VGL_LVL [4:0]				
Read/Write	NA	NA	NA	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	1	0	1	0	0

Name	Description
VGL_LVL [4:0]	Voltage setting for VGL -15V~-40V; 1V/Step Default: 0x14

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	-15V	0Bh	-26V	16h	-37V
01h	-16V	0Ch	-27V	17h	-38V
02h	-17V	0Dh	-28V	18h	-39V
03h	-18V	0Eh	-29V	19h	-40V
04h	-19V	0Fh	-30V		
05h	-20V	10h	-31V		
06h	-21V	11h	-32V		
07h	-22V	12h	-33V		
08h	-23V	13h	-34V		
09h	-24V	14h	-35V		
0Ah	-25V	15h	-36V		

VCOM Output Voltage (VCOM SETTING)

Address – 0x09h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VCOM_LVL [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	0	0	1	1

Name	Description
VCOM_LVL [7:0]	Voltage setting for VCOM 0V~-5V; 19.5mV/Step Default: 0x33

DAC	Voltage	DAC	Voltage	DAC	Voltage
00h	0.000V	16h	0.432V	2Eh	-0.9000V
01h	-0.0195V	17h	0.4515V	2Fh	-0.9195V
02h	-0.039V	18h	0.471V	30h	-0.9390V
03h	-0.0585V	19h	0.4905V	31h	-0.9585V
04h	-0.078V	1Ah	0.51V	32h	-0.9780V
05h	-0.0975V	1Bh	0.5295V	33h	-0.9975V
06h	-0.117V	1Ch	0.549V		
07h	-0.1365V	1Dh	0.5685V		
08h	-0.156V	1Eh	0.588V		
09h	-0.1755V	1Fh	0.6075V	F1	-4.7025V
0Ah	-0.195V	20h	0.627V	F2	-4.7220V
0Bh	-0.2145V	21h	0.6465V	F3	-4.7415V
0Ch	-0.234V	22h	0.666V	F4	-4.7610V
0Dh	-0.2535V	23h	0.6855V	F5	-4.7805V
0Eh	-0.273V	24h	0.705V	F6	-4.8000V
0Fh	-0.2925V	25h	0.7245V	F7	-4.8195V
10h	-0.312V	26h	0.744V	F8	-4.8390V
11h	-0.3315V	27h	0.7635V	F9	-4.8585V
12h	-0.351V	28h	0.783V	FA	-4.8780V
13h	-0.3705V	29h	0.8025V	FB	-4.8975V
14h	-0.39V	2Ah	0.822V	FC	-4.9170V
15h	-0.4095V	2Bh	0.8415V	FD	-4.9365V
16h	-0.429V	2Ch	0.8610V	FE	-4.9560V
17h	-0.4485V	2Dh	0.8805V	FF	-4.9755V

VBK Setting
Address – 0x0Ah

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VBK_DISC	CELL_SEL	VBK_EN	TDLY0	Reserved	VBK_CL_O	VBK_LVL[1:0]	
Read/Write	R/W	R/W	R/W	R/W	NA	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Name	Description
VBK_DISC	VBK_DISC Disable: 0; Enable: 1 Default: 0 Disable
CELL_SEL	CELL_SEL 0: 1 Cell, 1: 2 Cells Default: 00, 1 Cell
VBK_EN	VBK_EN 0: Disable, 1: Enable Default: 00,
TDLY0	TDLY0 0: 2ms, 1: 3ms Default: 00, 2ms
VBK_CL_O	VBK_Current Limit 0: 0.5A ; 1: 0.7A; Default: 00
VBK_LVL[1:0]	VBK_LVL 00: 1.2V; 01:1.8V; 10: 3.3V; 11: 3.3V Default: 00

Current Limit (Current limit: VN2, VP2, VN3, VP3)

Address – 0x0Bh

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VN2 Current Setting [1:0]		VP2 Current Setting [1:0]		VN3 Current Setting [1:0]		VP3 Current Setting [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	1	0	1	0	1	0

Name	Description
VN2 Current Setting [1:0]	VN2 Converter Current Limit Protection setting 00: 1.5A; 01: 2.5A; 10: 3.5A; 11: 4.5A Default: 3.5A
VP2 Current Setting [1:0]	VP2 Converter Current Limit Protection setting 00: 1.5A; 01: 2.5A; 10: 3.5A; 11: 4.5A Default: 3.5A
VN3 Current Setting [1:0]	VN3 Converter Current Limit Protection setting 00: 3A; 01: 4A; 10: 5A; 11: 6A Default: 5A
VP3 Current Setting [1:0]	VP3 Converter Current Limit Protection setting 00: 3A; 01: 4A; 10: 5A; 11: 6A Default: 5A

Soft start (Soft start time setting)

Address – 0x0Ch

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TSS1 [1:0]		TSS2 [2:0]			TSS3 [2:0]		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0

Name	Description
TSS1 [1:0]	VN1 、VP1 、VNEG1 、VPOS1 power on soft start time setting 00: 2ms, 01: 3ms, 10: 4ms, 11: 5ms Default: 2ms
TSS2 [2:0]	VN2 、VP2 、VNEG2 VPOS2 power on soft start time setting 000: 2ms, 001: 3ms, 010: 4ms, 011: 5ms, 100: 6ms, 101: 7ms, 110: 8ms, 111: 9ms Default: 2ms
TSS3 [2:0]	VN3 、VP3 、VNEG3 VPOS3 power on soft start time setting 000: 2ms, 001: 3ms, 010: 4ms, 011: 5ms, 100: 6ms, 101: 7ms, 110: 8ms, 111: 9ms Default: 4ms

Note 7: Tdly1+Tss2+Tdly3 > Tss3

Soft start and PWRON_DELAY (Soft start and Power ON delay time setting)

Address – 0x0Dh

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TSS4 [1:0]		TDLY1 [2:0]			DON'T Reserve		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	NA	NA	NA

Name	Description
TSS4 [1:0]	VGL and VGH power on soft start time setting 00: 2ms, 01: 3ms, 10: 4ms, 11: 5ms Default: 2ms
TDLY1 [2:0]	VN2 power on soft start delay time setting 0x00: 0.3ms, 0x01: 1ms, 0x02: 2ms, 0x03: 4ms, 0x04: 6ms, 0x05: 8ms, 0x06: 12ms, 0x07: 16ms Default: 0.3ms

PWRON_DELAY (Power ON delay time setting)

Address – 0x0Eh

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	TDLY3 [1:0]		TDLY4 [1:0]		TDLY5 [1:0]		TDLY6 [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Name	Description
TDLY3 [1:0]	VGL 、VCOM power on soft start delay time setting 00: 2ms, 01: 3ms, 10: 4ms, 11: 5ms Default: 2ms
TDLY4 [1:0]	VGH 、VNEG3 power on soft start delay time setting 00: 0.3ms, 01: 1ms, 10: 2ms, 11: 4ms Default: 0.3ms
TDLY5 [1:0]	VPOS3 、VNEG2 power on soft start delay time setting 00: 0.3ms, 01: 1ms, 10: 2ms, 11: 4ms Default: 0.3ms
TDLY6 [1:0]	VPOS2 power on soft start delay time setting 00: 0.3ms, 01: 1ms, 10: 2ms, 11: 4ms Default: 0.3ms

PWRON_DELAY (Power ON delay time setting)

Address – 0x0Fh

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGL_DIS	TDLY7 [2:0]			TDLY8 [1:0]		T_PC [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Name	Description
VGL_DIS	Discharge EN Control for VGL Discharge Function 0: Disable; 1: Enable Default: 0
TDLY7 [2:0]	VNEG1 power on soft start delay time setting 000: 0.3ms, 001: 2ms, 010: 4ms, 011: 6ms, 100: 8ms, 101: 10ms, 110: 12ms, 111: 16ms Default: 0.3ms
TDLY8 [1:0]	VPOS1 power on soft start delay time setting 00: 0.3ms, 01: 1ms, 10: 2ms, 11: 4ms Default: 0.3ms
T_PC [1:0]	VGH · VGLsoft start time setting 00: 1ms, 01: 2ms, 10: 3ms, 11: 4ms Default: 1ms

GATE DRIVER Control (EN_GD)

Address – 0x10h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve							EN_GD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	NA	NA	NA	NA	0

Name	Description
EN_GD	Enable Gate Drive Function for True Shutdown Disable: 0; Enable: 1 Default: Disable

Output level select

Address – 0x11h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Digital_ENTS	DON'T Reserve						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	NA	NA	NA	NA	NA	NA	NA

Name	Description
Digital_ENTS	Enable ENTS Function with This Bit 0: Disable, 1: Enable Default: 0, Disable

PMIC Function Control

Address – 0x12h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Power_DIS	MINI_ON_SEL	Night Mode	GD OFF, PCH SCP Linked	GD OFF, PCH UVP Linked	Reserved	GD OFF, NCH SCP Linked	GD OFF, NCH UVP Linked
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	NA	0	0

Name	Description
Power_DIS	Power Output Disable 0: Disable, 1: Enable Default: 0, Disable
MINI_ON_SELECT	Select MINI_ON_SELECT Enable or Disable 0: MINI_ON(PSM) Enable, 1: MINI_ON(PSM) Disable Default: 0, MINI_ON(PSM) Enable
Night Mode	Night Mode Function Control 0: Disable, 1: Enable Default: 0, Disable
GD OFF, PCH SCP Linked	Disable Gate Driver Function with VPOS1~3 SCP 0: Disable, 1: Enable Default: 0, Disable
GD OFF, PCH UVP Linked	Disable Gate Driver Function with VPOS1~3 UVP 0: Disable, 1: Enable Default: 0, Disable
GD OFF, NCH SCP Linked	Disable Gate Driver Function with VNEG1~3 SCP 0: Disable, 1: Enable Default: 0, Disable
GD OFF, NCH UVP Linked	Disable Gate Driver Function with VNEG1~3 UVP 0: Disable, 1: Enable Default: 0, Disable

DISA_DELAY
Address – 0x13h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	Don't Reserve				DISA_DELAY[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	NA	0	0	0	0

DAC	Delay Time	DAC	Delay Time
00h	0ms	08h	8ms
01h	1ms	09h	9ms
02h	2ms	0Ah	10ms
03h	3ms	0Bh	11ms
04h	4ms	0Ch	12ms
05h	5ms	0Dh	13ms
06h	6ms	0Eh	14ms
07h	7ms	0Fh	15ms

VGH Extension Time (VGH_EXT)
Address – 0x014h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve			VGH_EXT [4:0]				
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	0	0	0	0	0

DAC	Extension Time	DAC	Extension Time
00h	0ms	0Bh	550ms
01h	50ms	0Ch	600ms
02h	100ms	0Dh	650ms
03h	150ms	0Eh	700ms
04h	200ms	0Fh	750ms
05h	250ms	10h	800ms
06h	300ms	11h	850ms
07h	350ms	12h	900ms
08h	400ms	13h	950ms
09h	450ms	14h	1000ms
0Ah	500ms		

VGH Night Mode Setting (VGHNM_SETTING)

Address – 0x15h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve			VGHNM_SETTING [4:0]				
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	0	0	0	0	0

DAC	VGHNM Voltage	DAC	VGHNM Voltage
00h	2V	0Ah	7V
01h	2.5V	0Bh	7.5V
02h	3V	0Ch	8V
03h	3.5V	0Dh	8.5V
04h	4V	0Eh	9V
05h	4.5V	0Fh	9.5V
06h	5V	10h	10V
07h	5.5V		
08h	6V		
09h	6.5V		

VGL Extension Time (VGL_EXT)

Address – 0x16h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGL_EXT [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

DAC	Extension Time	DAC	Extension Time	DAC	Extension Time
00h	0ms	22h	1700ms	48h	3600ms
01h	50ms	23h	1750ms	49h	3650ms
02h	100ms	24h	1800ms	4Ah	3700ms
03h	150ms	25h	1850ms	4Bh	3750ms
04h	200ms	26h	1900ms		
05h	250ms	27h	1950ms		
06h	300ms	28h	2000ms		
07h	350ms	29h	2050ms		
08h	400ms	2Ah	2100ms		
09h	450ms	2Bh	2150ms		
0Ah	500ms	2Ch	2200ms		
0Bh	550ms	2Dh	2250ms		
0Ch	600ms	2Eh	2300ms		
....		2Fh	2350ms		
....		30h	2400ms		
....		31h	2450ms	7Ah	6100ms
....		32h	2500ms	7Bh	6150ms
1Fh	1550ms	45h	3450ms	7Ch	6200ms
20h	1600ms	46h	3500ms	7Dh	6250ms
21h	1650ms	47h	3550ms	7Eh	6300ms

VGHNM Extension Time (VGHNM_EXT)

Address – 0x17h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	VGHNM_EXT [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

DAC	Extension Time	DAC	Extension Time	DAC	Extension Time
00h	0ms	1Eh	1680ms	3Ch	3550ms
01h	50ms	1Fh	1740ms	3Dh	3620ms
02h	110ms	20h	1800ms	3Eh	3690ms
03h	160ms	21h	1860ms	3Fh	3750ms
04h	210ms	22h	1920ms	40h	3820ms
05h	270ms	23h	1980ms	41h	3890ms
06h	320ms	24h	2040ms	42h	3960ms
07h	380ms	25h	2100ms	43h	4030ms
08h	430ms	26h	2160ms	44h	4090ms
09h	490ms	27h	2220ms	45h	4160ms
0Ah	540ms	28h	2280ms	46h	4230ms
0Bh	600ms	29h	2340ms	47h	4300ms
0Ch	650ms	2Ah	2400ms	48h	4370ms
0Dh	710ms	2Bh	2460ms	49h	4440ms
0Eh	760ms	2Ch	2530ms	4Ah	4510ms
0Fh	820ms	2Dh	2590ms	4Bh	4580ms
10h	870ms	2Eh	2650ms	4Ch	4650ms
11h	930ms	2Fh	2710ms	4Dh	4720ms
12h	990ms	30h	2780ms	4Eh	4800ms
13h	1040ms	31h	2840ms	4Fh	4870ms
14h	1100ms	32h	2900ms	50h	4940ms
15h	1160ms	33h	2970ms	51h	5010ms
16h	1210ms	34h	3030ms	52h	5080ms
17h	1270ms	35h	3100ms	53h	5160ms
18h	1330ms	36h	3160ms	54h	5230ms
19h	1390ms	37h	3230ms	55h	5310ms
1Ah	1440ms	38h	3290ms	56h	5380ms
1Bh	1500ms	39h	3360ms	57h	5450ms
1Ch	1560ms	3Ah	3420ms	58h	5530ms
1Dh	1620ms	3Bh	3490ms	59h	5600ms

DAC	Extension Time	DAC	Extension Time	DAC	Extension Time
5Ah	5680ms	7Eh	8670ms	A2h	12350ms
5Bh	5760ms	7Fh	8760ms	A3h	12470ms
5Ch	5830ms	80h	8850ms	A4h	12580ms
5Dh	5910ms	81h	8950ms	A5h	12700ms
5Eh	5990ms	82h	9040ms	A6h	12820ms
5Fh	6060ms	83h	9130ms	A7h	12940ms
60h	6140ms	84h	9230ms	A8h	13060ms
61h	6220ms	85h	9320ms	A9h	13180ms
62h	6300ms	86h	9420ms	AAh	13300ms
63h	6380ms	87h	9510ms	ABh	13420ms
64h	6460ms	88h	9610ms	ACH	13540ms
65h	6540ms	89h	9710ms	ADH	13670ms
66h	6620ms	8Ah	9810ms	Aeh	13790ms
67h	6700ms	8Bh	9900ms	Afh	13920ms
68h	6780ms	8Ch	10000ms	B0h	14050ms
69h	6860ms	8Dh	10100ms	B1h	14170ms
6Ah	6940ms	8Eh	10200ms	B2h	14300ms
6Bh	7020ms	8Fh	10300ms	B3h	14430ms
6Ch	7110ms	90h	10400ms	B4h	14570ms
6Dh	7190ms	91h	10510ms	B5h	14700ms
6Eh	7270ms	92h	10610ms	B6h	14830ms
6Fh	7360ms	93h	10710ms	B7h	14970ms
70h	7440ms	94h	10820ms	B8h	15100ms
71h	7520ms	95h	10920ms	B9h	15240ms
72h	7610ms	96h	11030ms	BAh	15380ms
73h	7700ms	97h	11130ms	BBh	15520ms
74h	7780ms	98h	11240ms	BCh	15660ms
75h	7870ms	99h	11350ms	BDh	15800ms
76h	7960ms	9Ah	11460ms	BEh	15940ms
77h	8040ms	9Bh	11570ms	BFh	16090ms
78h	8130ms	9Ch	11680ms	C0h	16230ms
79h	8220ms	9Dh	11790ms	C1h	16380ms
7Ah	8310ms	9Eh	11900ms	C2h	16530ms
7Bh	8400ms	9Fh	12010ms	C3h	16680ms
7Ch	8490ms	A0h	12120ms	C4h	16830ms
7Dh	8580ms	A1h	12240ms	C5h	16980ms

DAC	Extension Time	DAC	Extension Time	DAC	Extension Time
C6h	17140ms	DAh	20590ms	EEh	24990ms
C7h	17290ms	DBh	20780ms	EFh	25240ms
C8h	17450ms	DCh	20980ms	F0h	25500ms
C9h	17610ms	DDh	21170ms	F1h	25760ms
CAh	17770ms	DEh	21370ms	F2h	26030ms
CBh	17930ms	DFh	21580ms	F3h	26300ms
CCh	18100ms	E0h	21780ms	F4h	26580ms
CDh	18260ms	E1h	21990ms	F5h	26860ms
CEh	18430ms	E2h	22200ms	F6h	27150ms
CFh	18600ms	E3h	22420ms	F7h	27440ms
D0h	18770ms	E4h	22640ms	F8h	27740ms
D1h	18940ms	E5h	22860ms	F9h	28050ms
D2h	19120ms	E6h	23080ms	FAh	28360ms
D3h	19290ms	E7h	23300ms	FBh	28670ms
D4h	19470ms	E8h	23530ms	FCH	28990ms
D5h	19650ms	E9h	23770ms	FDH	29320ms
D6h	19830ms	EAh	24000ms	FEH	29660ms
D7h	20020ms	EBh	24240ms	FFH	30000ms
D8h	20210ms	ECh	24490ms		
D9h	20390ms	EDh	24730ms		

Note 8: VGHNM_EXT value is depen on EIC formula as below:

$$VPDD_LEN(index) = \text{round}[-\tau \cdot \log(1 + index \cdot [\exp(-30/\tau) - 1]/255) \cdot 100] / 100 \text{ in s}$$

XON Delay Time (XON_DELAY)

Address – 0x18h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve	XON_DELAY [6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	0	0	0	0	0	0	0

Name	Description
XON_DELAY [6:0]	Night Mode Power OFF XON Delay Time Setting 0~500ms; 5ms/Step Default: 0ms

DAC	Delay Time	DAC	Delay Time	DAC	Delay Time
00h	0ms	1Ah	130ms		
01h	5ms	1Bh	135ms		
02h	10ms	1Ch	140ms		
03h	15ms	1Dh	145ms	4Eh	390ms
04h	20ms	1Eh	150ms	4Fh	395ms
05h	25ms	1Fh	155ms	50h	400ms
06h	30ms	20h	160ms	51h	405ms
07h	35ms	21h	165ms	52h	410ms
08h	40ms	22h	170ms	53h	415ms
09h	45ms	23h	175ms	54h	420ms
0Ah	50ms	24h	180ms	55h	425ms
0Bh	55ms	25h	185ms	56h	430ms
0Ch	60ms	26h	190ms	57h	435ms
0Dh	65ms	27h	195ms	58h	440ms
0Eh	70ms	28h	200ms	59h	445ms
0Fh	75ms	29h	205ms	5Ah	450ms
10h	80ms	2Ah	210ms	5Bh	455ms
11h	85ms	2Bh	215ms	5Ch	460ms
12h	90ms	2Ch	220ms	5Dh	465ms
13h	95ms	2Dh	225ms	5Eh	470ms
14h	100ms	2Eh	230ms	5Fh	475ms
15h	105ms	2Fh	235ms	60h	480ms
16h	110ms	30h	240ms	61h	485ms
17h	115ms	31h	245ms	62h	490ms
18h	120ms	32h	250ms	63h	495ms
19h	125ms	33h	255ms	64h	500ms

XON LEN Time (XON_LEN)

Address – 0x19h

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	XON_LEN [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Name	Description
XON_LEN [7:0]	XON LEN Time Setting 00h~FAh, 0ms~25000ms, 100ms/step Default: 0ms

DAC	LEN Time	DAC	LEN Time	DAC	LEN Time
00h	0ms	1Ah	2600ms		
01h	100ms	1Bh	2700ms		
02h	200ms	1Ch	2800ms		
03h	300ms	1Dh	2900ms	E4h	22800ms
04h	400ms	1Eh	3000ms	E5h	22900ms
05h	500ms	1Fh	3100ms	E6h	23000ms
06h	600ms	20h	3200ms	E7h	23100ms
07h	700ms	21h	3300ms	E8h	23200ms
08h	800ms	22h	3400ms	E9h	23300ms
09h	900ms	23h	3500ms	EAh	23400ms
0Ah	1000ms	24h	3600ms	EBh	23500ms
0Bh	1100ms	25h	3700ms	ECh	23600ms
0Ch	1200ms	26h	3800ms	EDh	23700ms
0Dh	1300ms	27h	3900ms	EEh	23800ms
0Eh	1400ms	28h	4000ms	EFh	23900ms
0Fh	1500ms	29h	4100ms	F0h	24000ms
10h	1600ms	2Ah	4200ms	F1h	24100ms
11h	1700ms	2Bh	4300ms	F2h	24200ms
12h	1800ms	2Ch	4400ms	F3h	24300ms
13h	1900ms	2Dh	4500ms	F4h	24400ms
14h	2000ms	2Eh	4600ms	F5h	24500ms
15h	2100ms	2Fh	4700ms	F6h	24600ms
16h	2200ms	30h	4800ms	F7h	24700ms
17h	2300ms	31h	4900ms	F8h	24800ms
18h	2400ms	32h	5000ms	F9h	24900ms
19h	2500ms	33h	5100ms	FAh	25000ms

Fault Flag

Address – 0x1Ah

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve			P or N	SCP or UVP	FAULT_CH [2:0]		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	0	0	0	0	0

Name	Description
P or N	Indicate Boost/Synchronous Buck or Buck-Boost Power Rail 1:P,Boost/Synchronous Buck; 0:N, Buck-Boost
SCP or UVP	Fault States 0: Under Voltage Protection; 1: Short Circuit Protection Default: 0:Under Voltage Protection
FAULT_CH [2:0]	Fault Flag Channel 000: Normal ; Default: 000

States	NEG Channel	P or N	SCP or UVP	FAULT_CH [2:0]			POS Channel	P or N	SCP or UVP	FAULT_CH [2:0]		
		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UVP	VN1	0	0	0	0	1	VP1	1	0	0	0	1
	VN2	0	0	0	1	0	VP2	1	0	0	1	0
	VN3	0	0	0	1	1	VP3	1	0	0	1	1
	VGL	0	0	1	0	0	VGH	1	0	1	0	0
	-	-	-	-	-	-	VBK	1	0	1	0	1
SCP	VN1	0	1	0	0	1	VP1	1	1	0	0	1
	VN2	0	1	0	1	0	VP2	1	1	0	1	0
	VN3	0	1	0	1	1	VP3	1	1	0	1	1
	VGL	0	1	1	0	0	VGH	1	1	1	0	0
	-	-	-	-	-	-	VBK	1	1	1	0	1

Fault Flag not shut down
Address – 0x1Bh

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Field Name	DON'T Reserve					OTP Flag	NA	PG Flag
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	NA	NA	NA	NA	NA	0	NA	0

Name	Description
OTP Flag	Over Temperature Protection Signal 0: Temperature normal, 1: Temperature fault Default: 0
PG Flag	Power Good Signal 0: PMIC normal operation, 1: PMIC power rail fault Default: 0

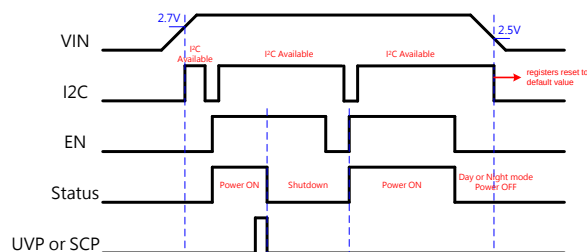
Application Information

Protection

The FP9937 monitors output voltages and die temperature. The device will take action if operating conditions are outside normal limits when the following is encountered:

- VPOSx/VNEGx Under Voltage Protection (UVP)
- VPOSx/VNEGx Short Circuit Protection (SCP)
- IC Over-Temperature Protection (OTP)

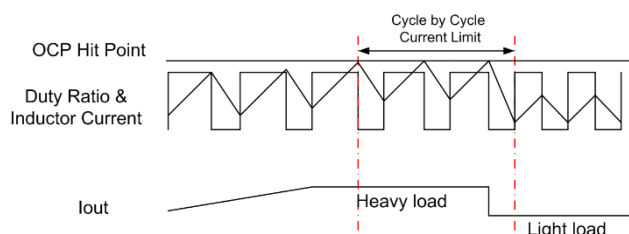
It shuts down all power rails and enters Shutdown mode. Power rails cannot be re-enabled unless the EN pin has been from low to high. As below figure.



Note 9: VPOSx/VNEGx, x means 1,2,3.

Over Current Protection (OCP)

The FP9937 over current protection function is implemented using cycle-by-cycle current limit architecture. Inductor current is monitored via the non-synchronous regulator's MOSFET or the synchronous regulator's high-side MOSFET. When the load current increases, the inductor current also increases. When the peak inductor current reaches the current limit threshold, the output voltage starts to drop. When the over current condition is removed, the output voltage returns to the regulated value.



Under Voltage Protection (UVP)

If VPOSx and VNEGx output voltage is between 80% and 40% of the setting voltage and reach 40ms, the IC will shut-down immediately. Once the device re-power on, IC will return to normal operation.

Short Circuit Protection (SCP)

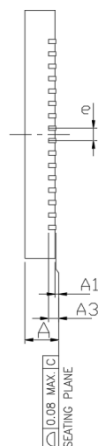
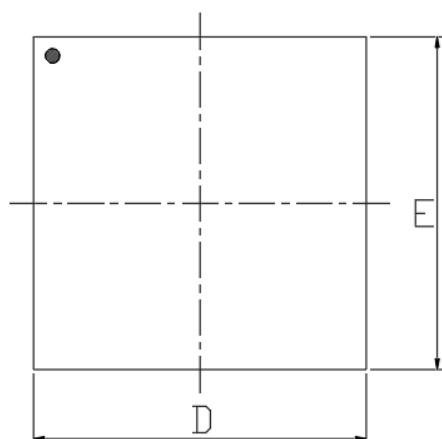
If VPOSx and VNEGx output voltage is below 40% of the setting voltage and reach 20us, the IC will shut-down immediately. Once the device re-power on, IC will return to normal operation.

Over-Temperature Protection

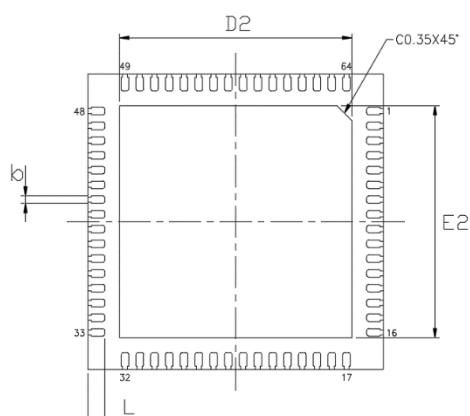
The FP9937 provides Over-Temperature Protection (OTP) to prevent excessive power dissipation from overheating the IC. When the junction temperature exceeds $T_J=140^{\circ}\text{C}$, a thermal sensor activates the fault protection, which shuts down the IC, allowing the IC to cool. Once the device re-power on, IC will return to normal operation.

Outline Information

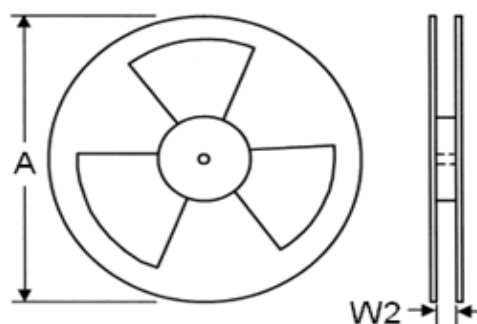
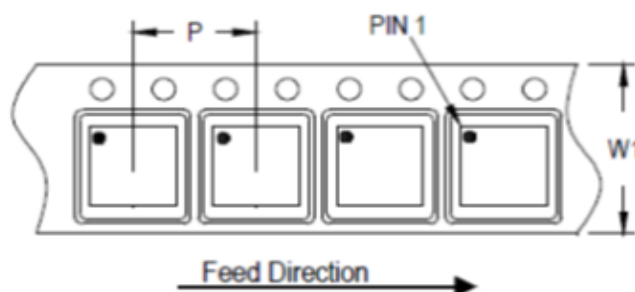
TQFN-64L (7mmx7mm) (pitch 0.35mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
E	6.90	7.10
D	6.90	7.10
L	0.30	0.50
b	0.13	0.25
e	0.35 BSC	
E2	5.40	5.60
D2	5.40	5.60



Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
16	12	13	330	16.4	400~1000	3,000

Revision History

Date	Revision	Change List
MAY-2025	0.1	Initial
OCT-2025	0.2	Add input voltage range of 1S1P and 2S1P battery in EC table
OCT-2025	0.3	Revise VPOS1/VNEG1 range. Add VPOS/VNEG polarity setting
NOV-2025	0.4	Revise power on sequence add RST sequence
NOV-2025	0.5	Revise application circuit. Add register address map default value
DEC-2025	0.6	Voltage Default Setting revise, Protection mechanism explain
JAN-2026	0.7	Add OCP mechanism explain. Pwr seq revise. Add Note 7 about Tss3
MAR-2026	0.8	Pwr seq revise

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.