18V, 5.5A Synchronous Step-Down DC/DC Converter

Description

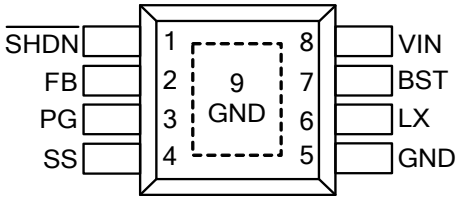
The FR9855 is a synchronous step-down DC/DC converter with fast constant on time (FCOT) mode control. The device provides 4.5V to 18V input voltage range and 5.5A continuous load current capability. Operation frequency depends on Input and output voltage condition. At light load condition, the FR9855 can operate at power saving mode to support high efficiency and reduce power loss.

The FR9855 fault protection includes cycle-by-cycle current limit, short circuit protection, UVLO and thermal shutdown. The soft-start function prevents inrush current at turn-on. The FR9855 use fast constant on time control that provides fast transient response, the noise immunity and all kinds of very low ESR output capacitor for ensuring performance stabilization.

The FR9855 is offered in SOP-8 (Exposed Pad) and TDFN-10 (3mm x 3mm) packages, which provides good thermal conductance.

Pin Assignments

SP Package (SOP-8 Exposed Pad)



DA Package (TDFN-10)(3mm x 3mm)

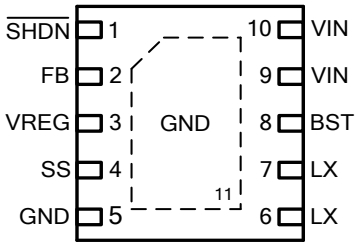


Figure 1. Pin Assignments of FR9855

Features

- Low $R_{DS(ON)}$ Integrated Power MOSFET (70mΩ/38mΩ)
- Wide Input Voltage Range: 4.5V to 18V
- Output Voltage Range: 0.765V to 8V
- 5.5A Output Current
- FCOT Mode Enables Fast Transient Response
- Pseudo 630kHz Frequency
- Power Good Function (for FR9855SP Only)
- Input Under Voltage Lockout
- Adjustable Soft Start Function
- Cycle-by-Cycle Current Limit
- Hiccup Short Circuit Protection
- Over Temperature Protection with Auto Recovery
- SOP-8 Exposed Pad and TDFN-10(3mmx3mm) Packages

Applications

- STB (Set-Top-Box)
- LCD Display, TV
- Distributed Power System
- Networking, XDSL Modem

Ordering Information

FR9855□

Package Type
SP: SOP-8 (Exposed Pad)
DA: TDFN-10(3mm x 3mm)

Typical Application Circuit

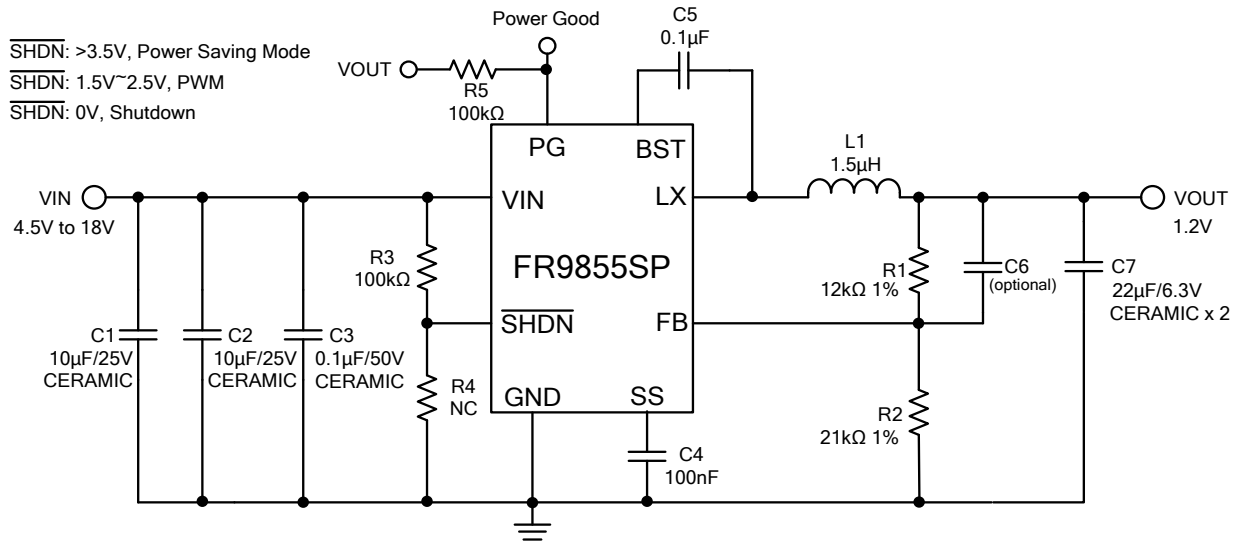


Figure 2. Application Circuit for SOP-8 Exposed Pad Package

V_{IN}=12V, the recommended BOM list is as below.

V_{OUT}	C1	R1	R2	C2	C6	L1	C7
1.05V	10μF MLCC	7.87kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
1.2V	10μF MLCC	12kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
1.8V	10μF MLCC	28kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
3.3V	10μF MLCC	69.8kΩ	21kΩ	10μF MLCC	5pF~33pF	2.2μH	22μF MLCC x2
5V	10μF MLCC	118kΩ	21kΩ	10μF MLCC	5pF~33pF	3.3μH	22μF MLCC x2

Table 1. Recommended Component Values

Typical Application Circuit (Continued)

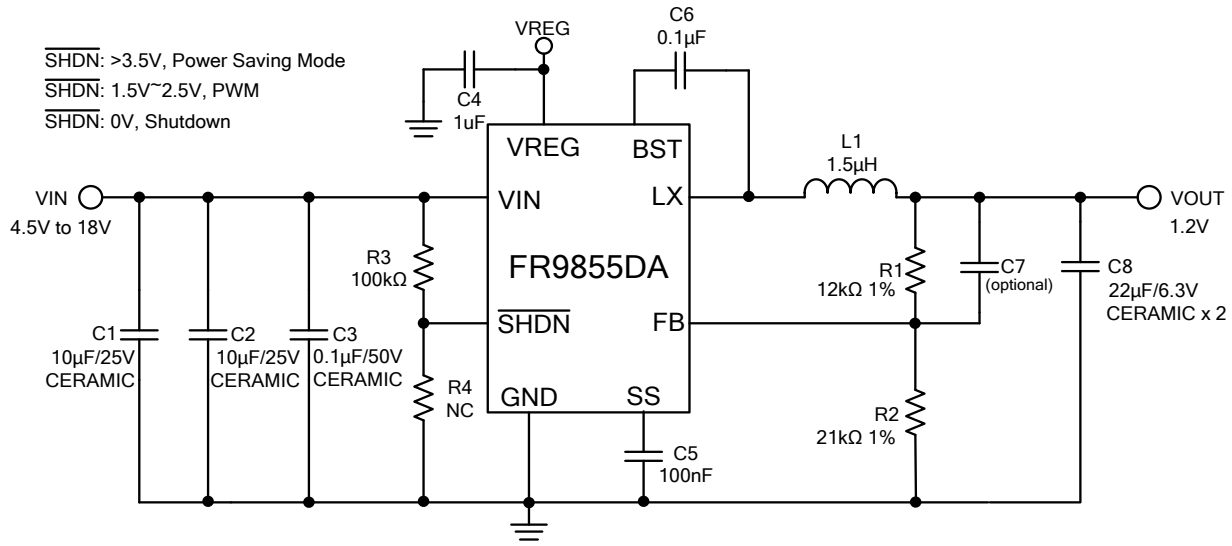


Figure 3. Application Circuit for TDFN-10 Package

V_{IN}=12V, the recommended BOM list is as below.

V_{OUT}	C1	R1	R2	C2	C7	L1	C8
1.05V	10μF MLCC	7.87kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
1.2V	10μF MLCC	12kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
1.8V	10μF MLCC	28kΩ	21kΩ	10μF MLCC	5pF~33pF	1.5μH	22μF MLCC x2
3.3V	10μF MLCC	69.8kΩ	21kΩ	10μF MLCC	5pF~33pF	2.2μH	22μF MLCC x2
5V	10μF MLCC	118kΩ	21kΩ	10μF MLCC	5pF~33pF	3.3μH	22μF MLCC x2

Table 2. Recommended Component Values

Functional Pin Description

Pin Name	Pin No. (SOP-8EP)	Pin No. (TDFN3x3-10)	Pin Function
$\overline{\text{SHDN}}$	1	1	This pin includes enable the converter on/off, and select operation mode (The mode setting, please refer to the following page 11). Connect VIN with a 100kΩ resistor for self-startup and operate in power saving mode.
FB	2	2	Voltage feedback input pin. Connect FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.765V.
PG	3	x	Open drain power good output.
SS	4	4	Soft-start pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period.
GND	5	5	Ground pin.
LX	6	6,7	Power switching node. Connect an external inductor to this switching node.
BST	7	8	High side gate drive boost pin. The boost capacitor selection rating between 0.1uF to 1uF which must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS.
VIN	8	9,10	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
Exposed Pad	9	11	Ground pin. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation.
VREG	x	3	Internal regulator output. Connect a 1uF capacitor to GND to stabilize the internal regulator voltage.

Block Diagram

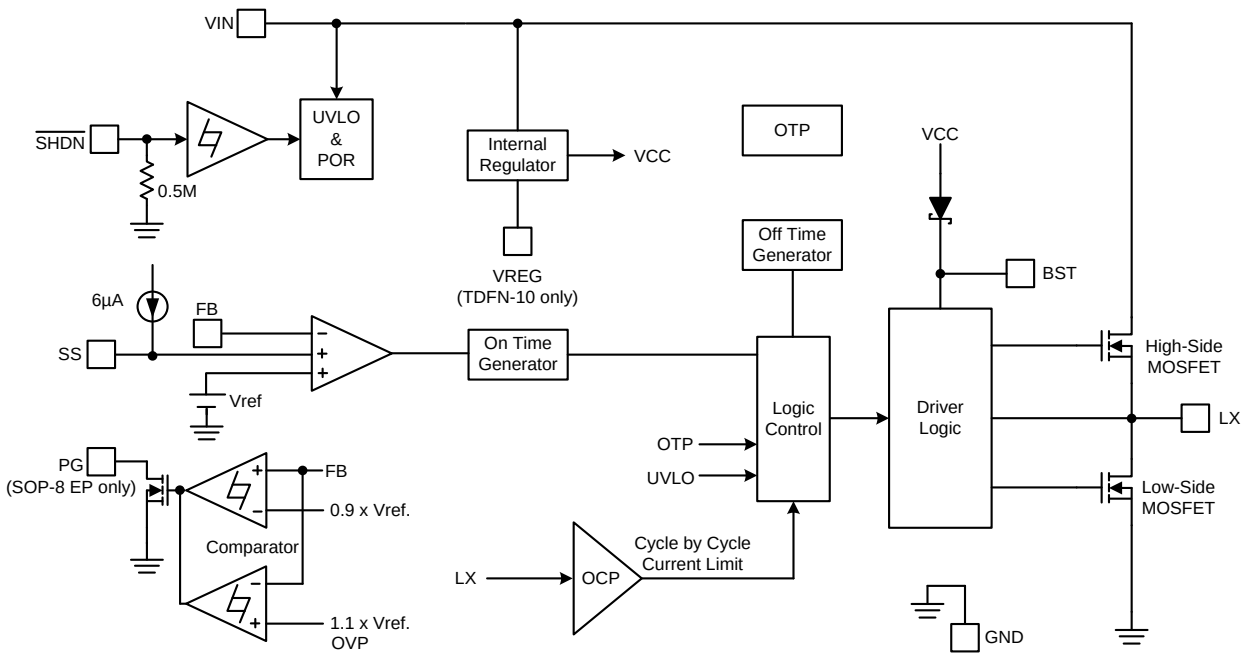


Figure 4. Block Diagram of FR9855

Absolute Maximum Ratings (Note 1)

- Supply Voltage V_{IN} ---------- -0.3V to +20V
- Enable Voltage $V_{\overline{SHDN}}$ ---------- -0.3V to +20V
- LX Voltage V_{LX} ---------- -0.3 to V_{IN} +0.3V
- Dynamic LX Voltage in 15ns Duration---------- -5V to V_{IN} +5V
- BST Pin Voltage V_{BST} ---------- -0.3V to V_{LX} +6.5V
- All Other Pins Voltage ---------- -0.3V to +6V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Package Thermal Resistance, (θ_{JA}) (Note 2)

  SOP-8 (Exposed Pad) ---------- 60°C/W

  TDFN-10 (3mmx3mm) ---------- 65°C/W
- Package Thermal Resistance, (θ_{JC}) (Note 2)

  SOP-8(Exposed Pad) ---------- 15°C/W

  TDFN-10(3mmx3mm) ---------- 30°C/W

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity 4-layer board of JEDEC-51-7. θ_{JC} is measured at the exposed pad. The thermal resistance greatly varies with layout, copper thickness, number of layers and PCB size.

Recommended Operating Conditions

- Supply Voltage V_{IN} ---------- +4.5V to +18V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Quiescent Current	I_{DDQ}	$V_{\overline{SHDN}}$=5V, V_{FB}=1V		0.6	1	mA
V_{IN} Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}$=0V		1	10	μA
Feedback Voltage	V_{FB}	4.5V≦V_{IN}≦18V	0.75	0.765	0.78	V
Feedback Input Current	I_{FB}	V_{FB}=1V		0.01	0.1	μA
High-Side MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			70		mΩ
Low-Side MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			38		mΩ
Current Limit (Note 3)	I_{LIMIT}			6.8		A
On Time (Note 3)	T_{ON}	V_{IN}=12V, V_{OUT}=1.05V		155		ns
Minimum Off Time	$T_{OFF(MIN)}$	V_{FB}=0.6V		250		ns
Input Supply Voltage UVLO Threshold	$V_{UVLO(Vth)}$	V_{IN} Rising		4.1		V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$			0.35		V
Soft Start Charge Current	I_{SS}	V_{SS}=0V		6		μA
$\overline{SHDN}$ Input Low Voltage	$V_{\overline{SHDN}(L)}$				0.5	V
$\overline{SHDN}$ Input High Voltage	$V_{\overline{SHDN}(H)}$		1.5			V
REG Output Voltage	V_{REG}	6V≦V_{IN}≦18V, FR9855DA		4.1		V
REG Output Current	I_{REG}	V_{REG}=4.1V, FR9855DA		10		mA
Power Good Threshold (Note 3)	V_{PG}	V_{FB} Rising, FR9855SP		90		%
		V_{FB} Falling, FR9855SP		85		
Power Good Sink Current	I_{PG}	V_{PG}=0.5V, FR9855SP		4		mA
Thermal Shutdown Threshold (Note 3)	T_{SD}			160		°C
Thermal Shutdown Hysteresis (Note 3)	T_{HYS}			30		°C

Note 3: Not production tested.

Typical Performance Curves

V_{IN}=12V, V_{OUT}=1.2V, C1=10μFx2, C7=22μFx2, L1=1.5μH, T_A=+25°C, unless otherwise noted. This is measured by using FR9855SP.

V_{OUT}=1.05V

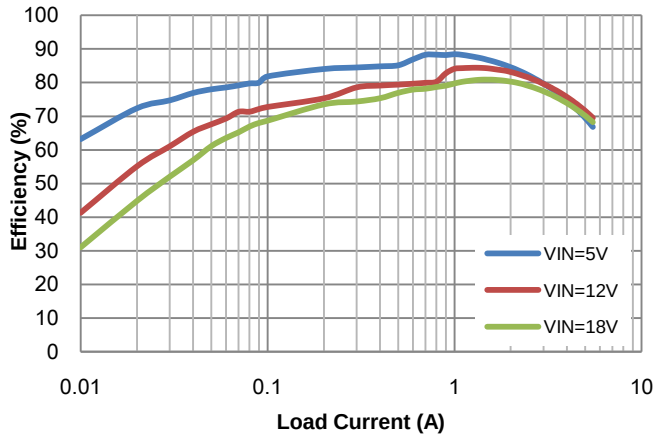


Figure 5. Efficiency vs. Load Current

V_{OUT}=1.2V

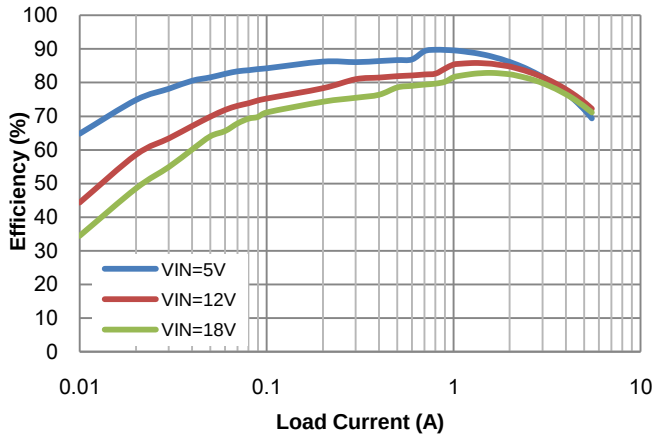


Figure 6. Efficiency vs. Load Current

V_{OUT}=3.3V

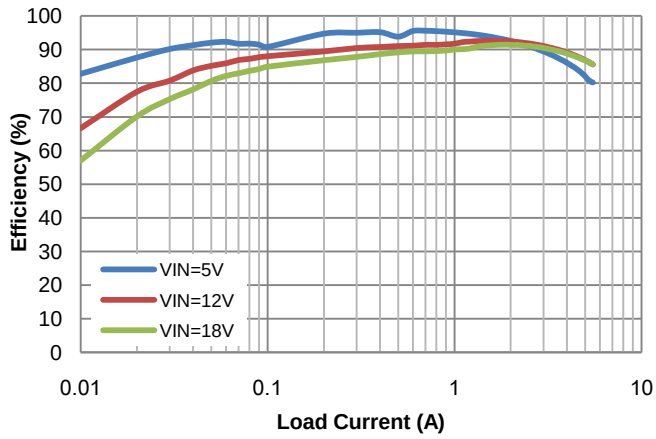


Figure 7. Efficiency vs. Load Current

V_{OUT}=5V

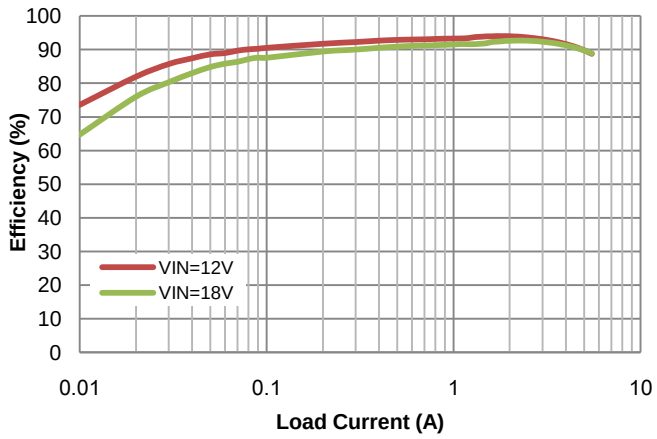


Figure 8. Efficiency vs. Load Current

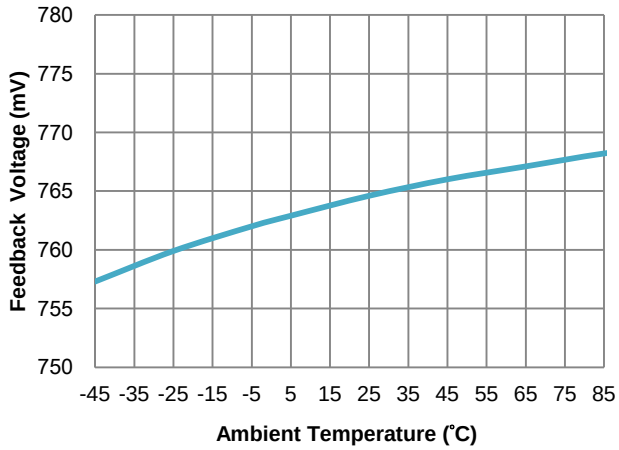


Figure 9. Feedback Voltage vs. Ambient Temperature

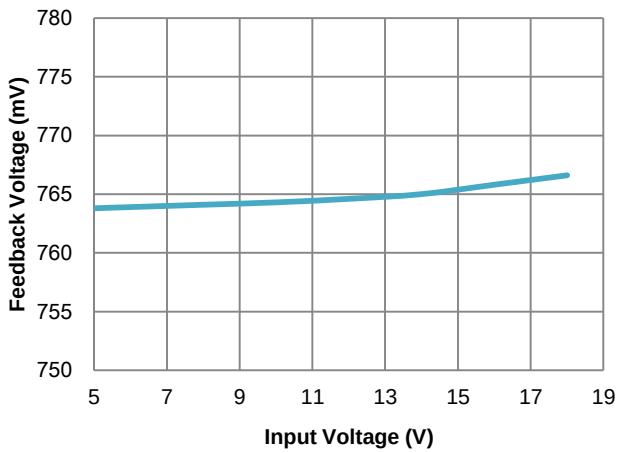


Figure 10. Feedback Voltage vs. Input Voltage

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=1.2V, C1=10μFx2, C7=22μFx2, L1=1.5μH, T_A=+25°C, unless otherwise noted. This is measured by using FR9855SP.

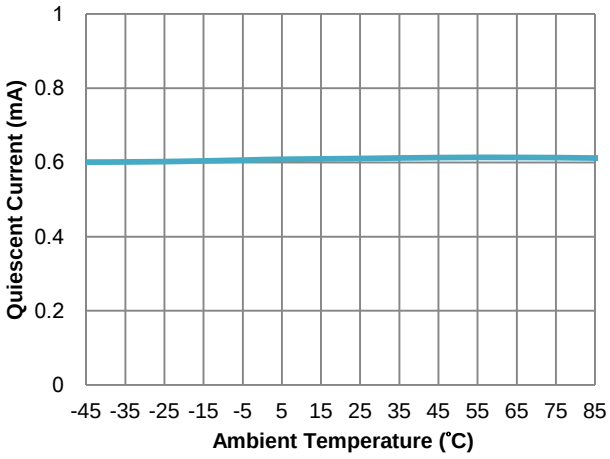


Figure 11. Quiescent Current vs. Ambient Temperature

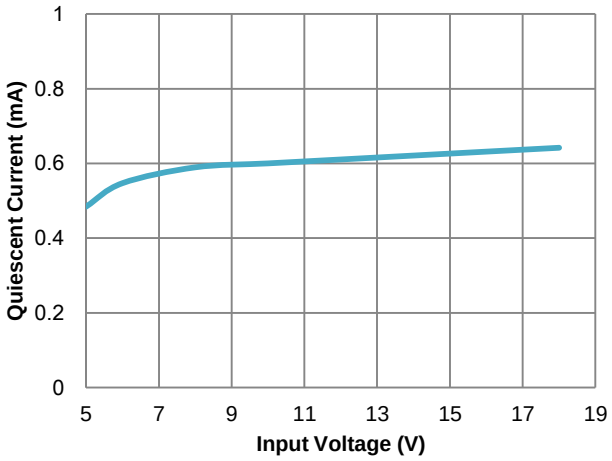


Figure 12. Quiescent Current vs. Input Voltage

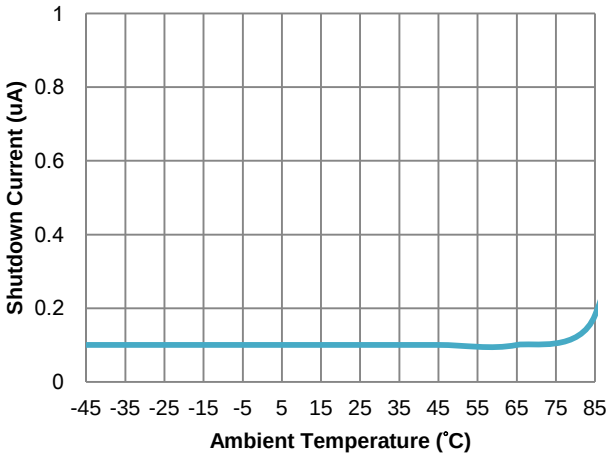


Figure 13. Shutdown Current vs. Ambient Temperature

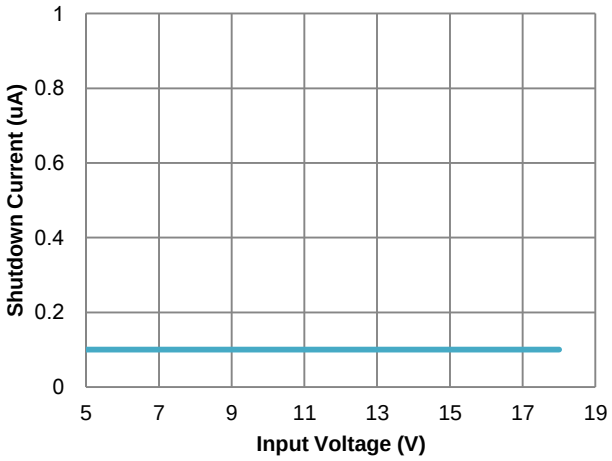


Figure 14. Shutdown Current vs. Input Voltage

V_{IN}=12V, $V_{\overline{SHDN}}$=2V V_{OUT}=1V, L=1.5μH

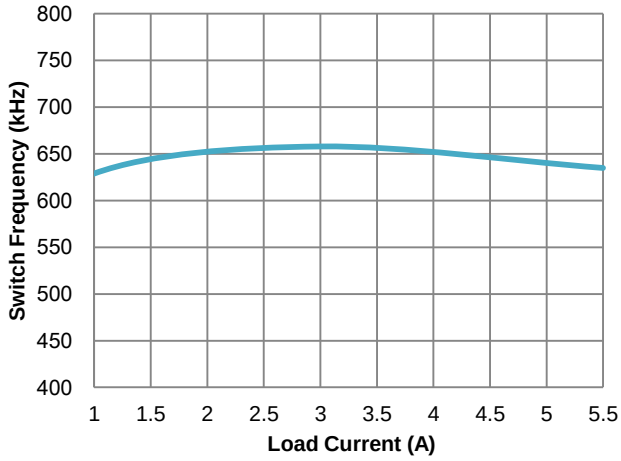


Figure 15. Switch Frequency vs. Load Current

V_{IN}=12V, $V_{\overline{SHDN}}$=2V V_{OUT}=5V, L=3.3μH

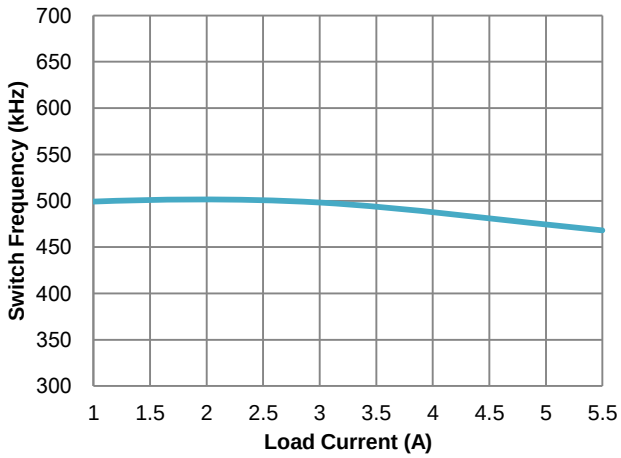


Figure 16. Switch Frequency vs. Load Current

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=1.2V, C1=10μFx2, C7=22μFx2, L1=1.5μH, T_A=+25°C, unless otherwise noted. This is measured by using FR9855SP.

I_{OUT}=0A

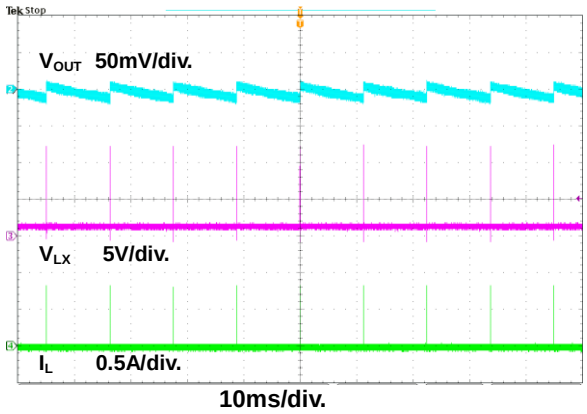


Figure 17. DC Ripple Waveform

I_{OUT}=5.5A

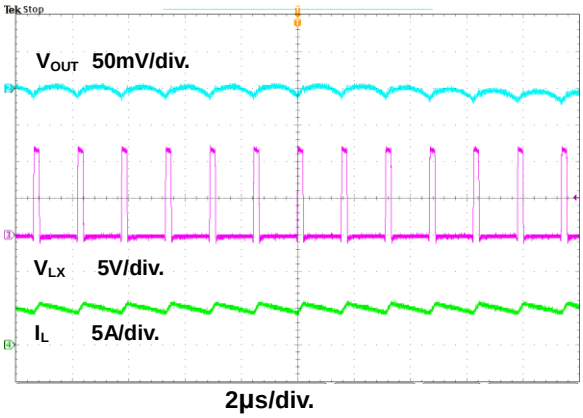


Figure 18. DC Ripple Waveform

I_{OUT}=0A

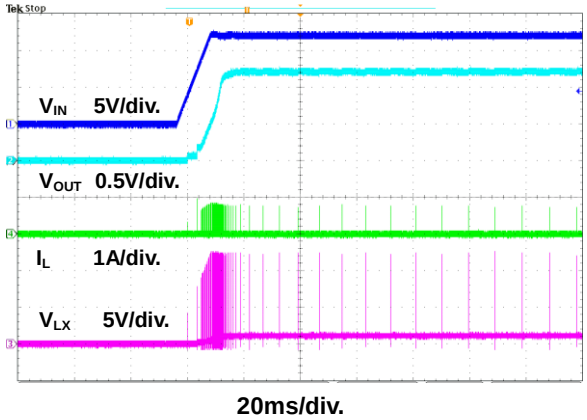


Figure 19. Startup Through Power Supply Waveform

I_{OUT}=5.5A

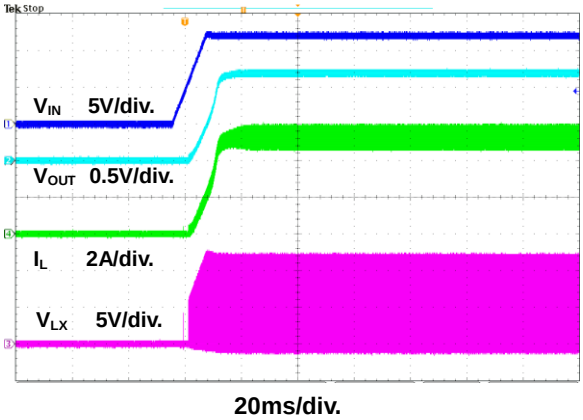


Figure 20. Startup Through Power Supply Waveform

I_{OUT}=0A

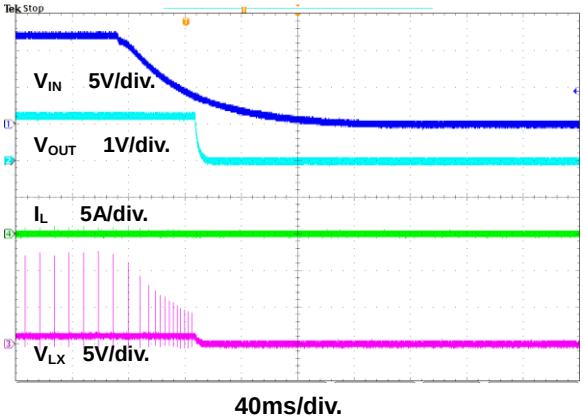


Figure 21. Shutdown Through Power Supply Waveform

I_{OUT}=5.5A

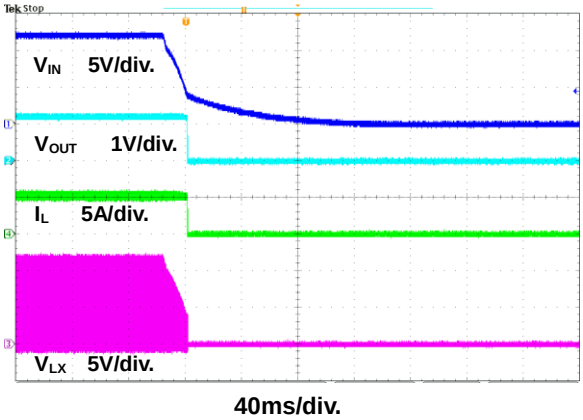


Figure 22. Shutdown Through Power Supply Waveform

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=1.2V, C1=10μFx2, C7=22μFx2, L1=1.5μH, T_A=+25°C, unless otherwise noted. This is measured by using FR9855SP.

I_{OUT}=0A

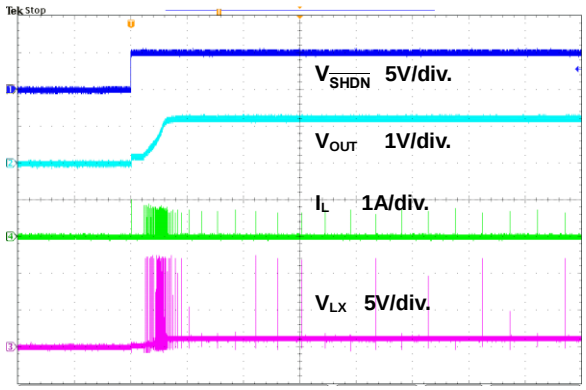


Figure 23. Startup Through $\overline{SHDN}$ Waveform

I_{OUT}=5.5A

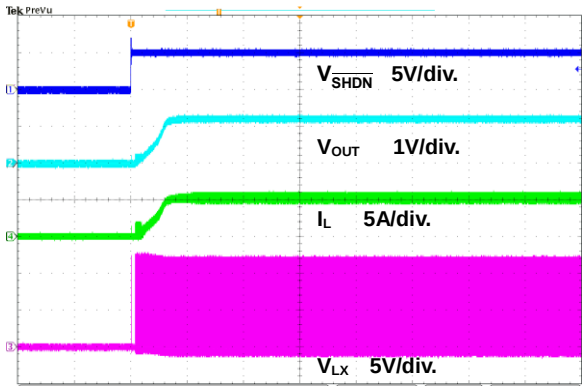


Figure 24. Startup Through $\overline{SHDN}$ Waveform

I_{OUT}=0A

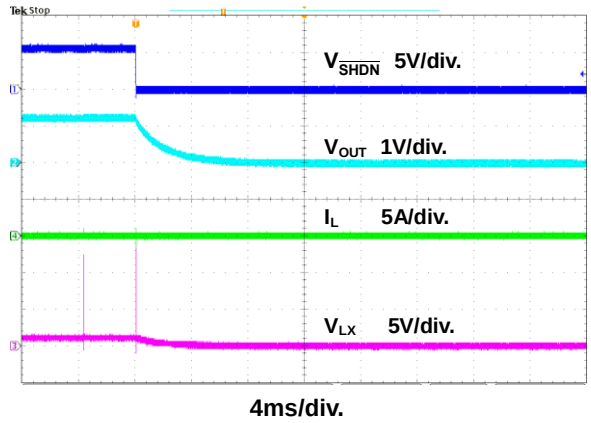


Figure 25. Shutdown Through $\overline{SHDN}$ Waveform

I_{OUT}=5.5A

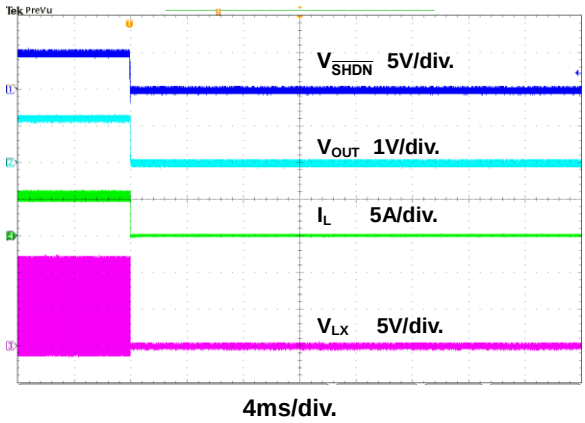


Figure 26. Shutdown Through $\overline{SHDN}$ Waveform

I_{OUT}=0.1A~5.5A

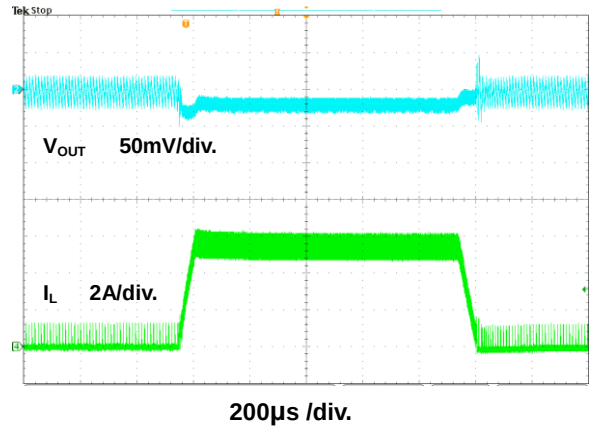


Figure 27. Load Transient Waveform

Function Description

The FR9855 is a synchronous step-down DC/DC converter with fast constant on time (FCOT) mode control. It has integrated high-side (70mΩ, typ) and low-side (38mΩ, typ) power switches, and provides 5.5A continuous load current. It regulates input voltage from 4.5V to 18V, and down to an output voltage as low as 0.765V. Using FCOT control scheme provides fast transient response, which can minimize the component size without additional external compensation network.

Enable/Mode

The FR9855 $\overline{SHDN}$ pin includes enable and mode function. Enable function provides digital control to turn on/off the converter. When the voltage of $\overline{SHDN}$ exceeds the threshold voltage, the converter starts the soft start function. If the $\overline{SHDN}$ pin voltage is below than the shutdown threshold voltage, the converter will turn into the shutdown mode and the shutdown current will be smaller than 1μA. The mode function can be selected in PWM or power saving mode. The mode setting can refer to following table.

$\overline{SHDN}$	Mode
>3.5V	Power Saving Mode
1.5V~2.5V	PWM
0V	Shutdown

For auto start-up operation, connect $\overline{SHDN}$ to VIN through a 100kΩ resistor, and the converter can automatically enter power saving mode.

Soft Start

The FR9855 employs adjustable soft start function to reduce input inrush current during start up. When the device turns on, a 6μA current begins charging the capacitor which is connected from SS pin to GND. The equation for the soft start time is shown as below:

$$T_{SS}(ms)=\frac{C_{SS}(nF)\times V_{FB}}{I_{SS}(\mu A)}$$

The V_{FB} voltage is 0.765V and the I_{SS} current is 6μA. If a 100nF capacitor is connected from SS pin to GND, the soft-start time will be 12.75ms.

Input Under Voltage Lockout

When the FR9855 is power on, the internal circuits are held inactive until V_{IN} voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 350mV (typ).

Over Current Protection

The FR9855 over current protection function is implemented using cycle-by-cycle current limit architecture. The inductor current is monitored by Low-side MOSFET. When the load current increases, the inductor current also increases. When the valley inductor current reaches the current limit threshold, the output voltage starts to drop. When the over current condition is removed, the output voltage returns to the regulated value.

Short Circuit Protection

The FR9855 provides short circuit protection function to prevent the device damage from short condition. When the short condition occurs and the feedback voltage drops lower than 0.33V, the oscillator frequency will be reduced naturally and hiccup mode will be triggered to prevent the inductor current increasing beyond the current limit. Once the short condition is removed, the frequency will return to normal.

Over Temperature Protection

The FR9855 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 30°C (typ).

Power Good Signal Output (PG)

PG pin is an open-drain output and requires a pull up resistor. PG is actively held low in soft-start, standby, OVP and shutdown. It is released when the output voltage rises above 90% of nominal regulation point.

Output Over Voltage Protection

When the FB pin voltage exceeds 110%*V_{ref}, the output over voltage protection function will be triggered. The high-side/low-side MOSFET turn off and PG signal pull low.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.765V. Thus the output voltage equation is:

$$V_{OUT}=0.765V\times\left(1+\frac{R1}{R2}\right)$$

Table 3 lists recommended values of R1 and R2 for most used output voltage.

Table 3 Recommended Resistance Values

V_{OUT}	R1	R2
5V	118kΩ	21kΩ
3.3V	69.8kΩ	21kΩ
1.8V	28kΩ	21kΩ
1.2V	12kΩ	21kΩ
1.05V	7.87kΩ	21kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

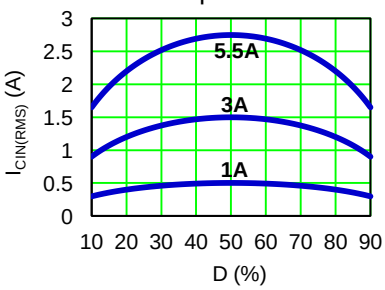
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{CIN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



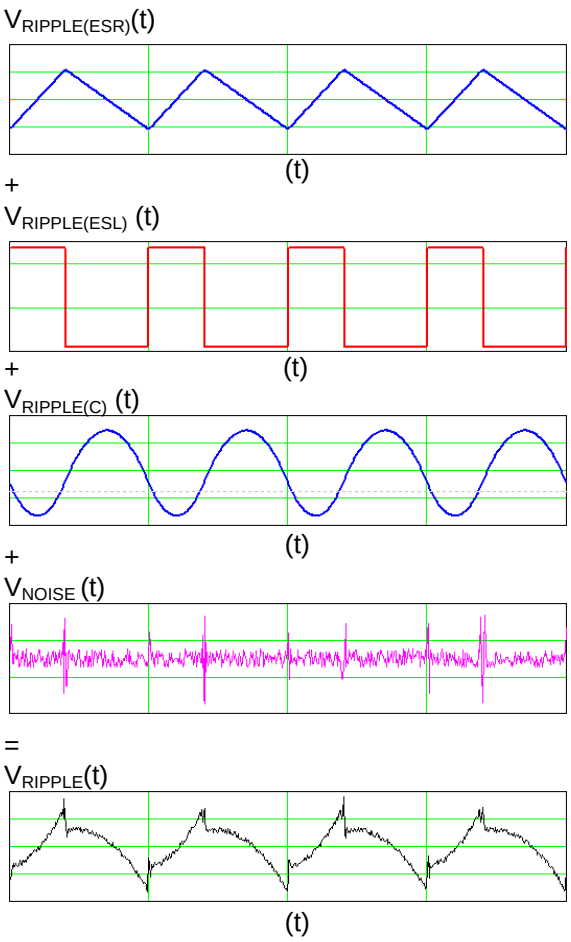
A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.



Application Information (Continued)

$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

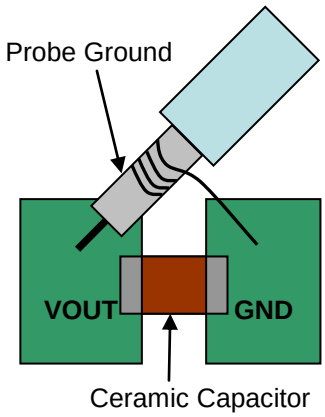
$$V_{RIPPLE(ESL)}=\frac{ESL}{L}\times V_{IN}$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC}^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirement. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminating noise.



Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

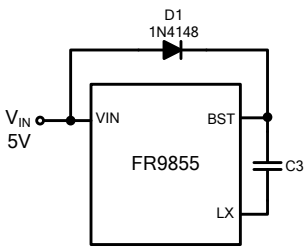
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times \Delta I_L}$$

External Diode Selection

For 5V input applications, it is recommended to add an external boost diode. This helps improving the efficiency. The boost diode can be a low cost one such as 1N4148.



REG Capacitor Selection

Connect a 1uF ceramic capacitor between the REG and GND, This helps stabilize the internal regulator voltage.

Application Information (Continued)

PCB Layout Recommendation

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

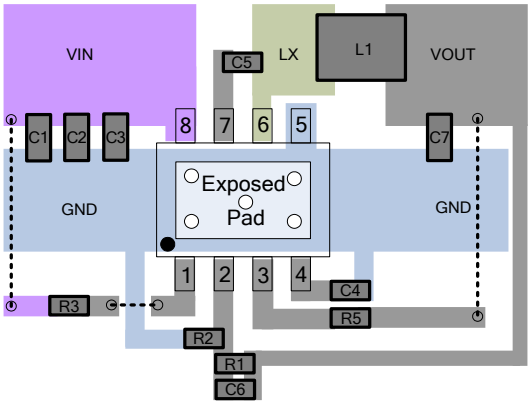


Figure 28. Recommended PCB Layout Diagram for SP Package

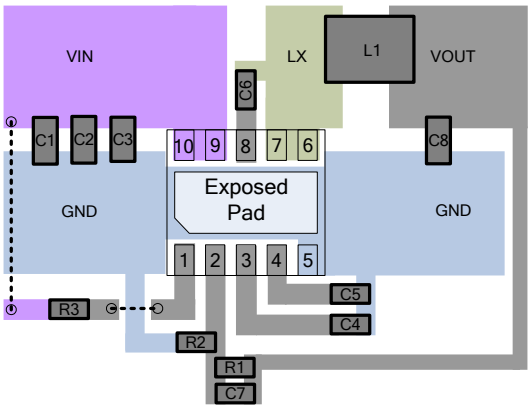
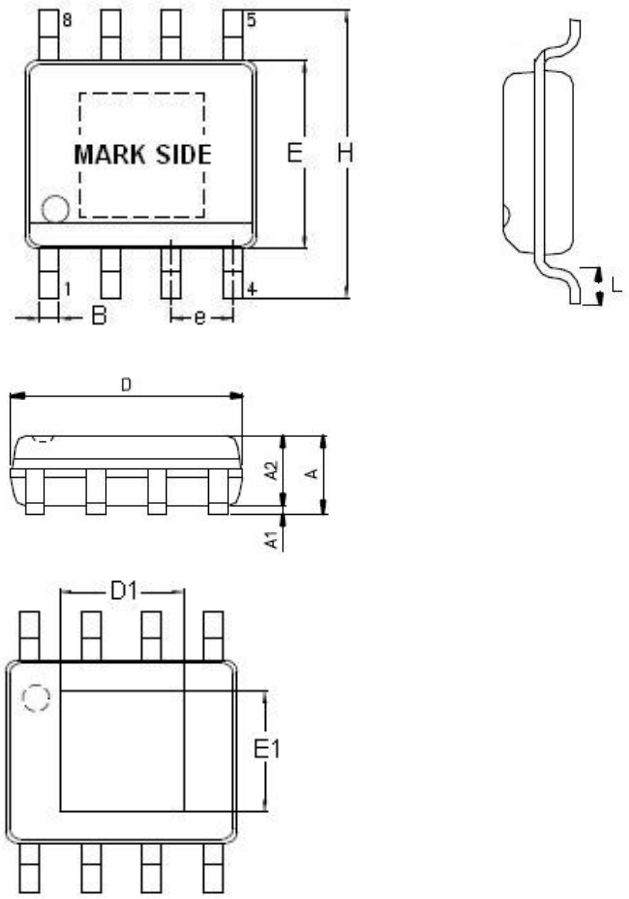


Figure 29. Recommended PCB Layout Diagram for DA Package

Outline Information

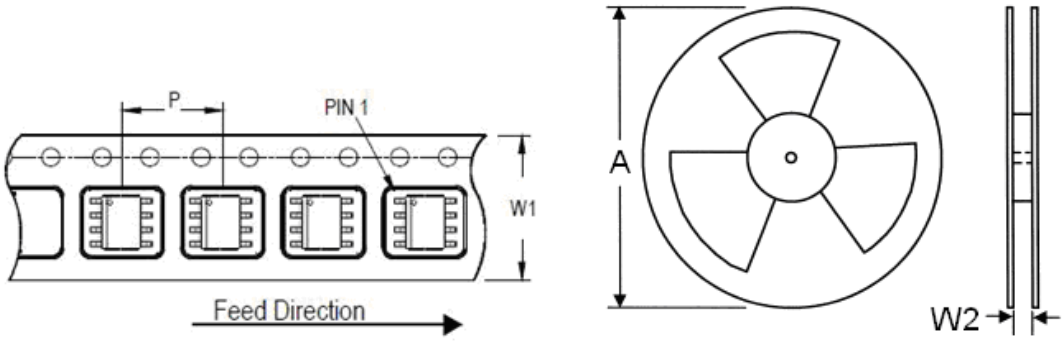
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note: Followed From JEDEC MO-012-E.

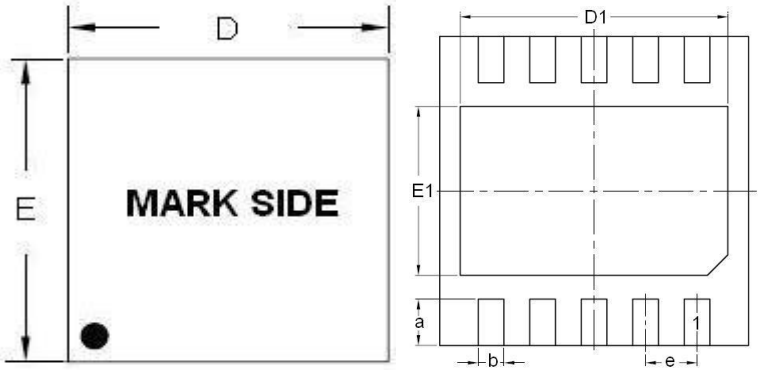
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

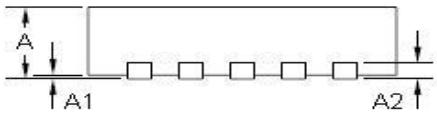
Outline Information (Continued)

TDFN-10 3mm x 3mm (pitch 0.5 mm) Package (Unit: mm)

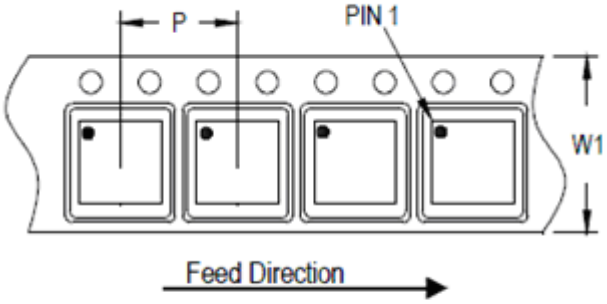


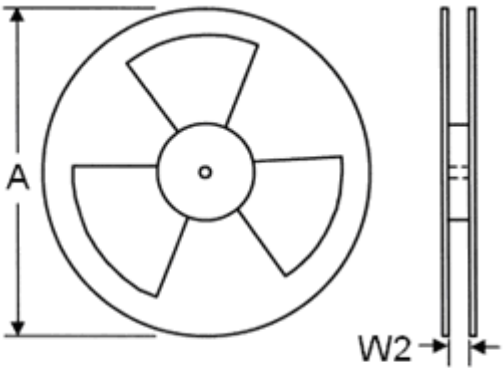
SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	2.95	3.05
E	2.95	3.05
a	0.30	0.50
b	0.18	0.30
e	0.45	0.55
D1	2.20	2.70
E1	1.40	1.75

Note: Followed From JEDEC MO-229F.



Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

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