3A Ultra Low Dropout Linear Regulator

Description

The FP6145 is a 3A ultra low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The FP6145 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent wrong operations. A thermal shutdown and current limit functions protect the device against thermal and current over-loads. A PG indicates the output status with time delay which is set internally. It can control other converter for power sequence. The FP6145 can be enabled by other power system. Pulling and holding the EN pin below 0.4V shuts off the output.

The FP6145 is available in SOP-8 (Exposed Pad) and TDFN-10L (3mmx3mm) packages which features small size as an exposed pad to reduce the junction-to-case resistance.

Features

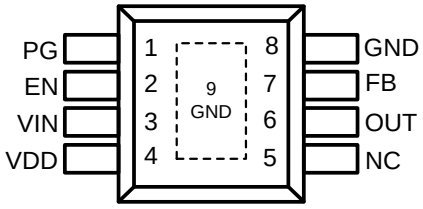
- Ultra Low Dropout-0.23V (Typical) at 3A Output Current
- Low ESR Output Capacitor (Multi-Layer Chip Capacitors (MLCC)) Applicable
- 0.8V Reference Voltage
- Fast Transient Response
- Adjustable Output Voltage by External Resistors
- Power-On-Reset Monitoring on Both VDD and VIN Pins
- Internal Soft-Start
- Under-Voltage Protection
- Current-Limit and Thermal Shutdown Protection
- Power Good Function
- RoHS Compliant and Halogen Free
- TSCA(USA) Compliant
- SOP-8 (Exposed Pad) and TDFN-10L (3mmx3mm) Packages

Applications

- LCD Monitor
- PC Motherboard/NB
- Graphic Card
- DVD-Video Player
- ADSL Modem
- Printer and other Peripheral Equipment

Pin Assignment

SP Package: SOP-8 (Exposed Pad)



DA Package: TDFN-10L (3mmx3mm)

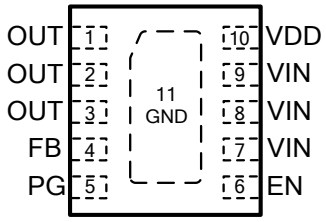
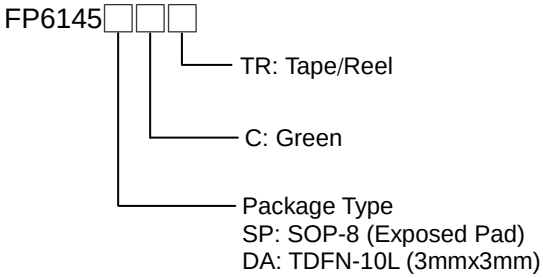


Figure 1. Pin Assignment of FP6145

Ordering Information



Typical Application Circuit

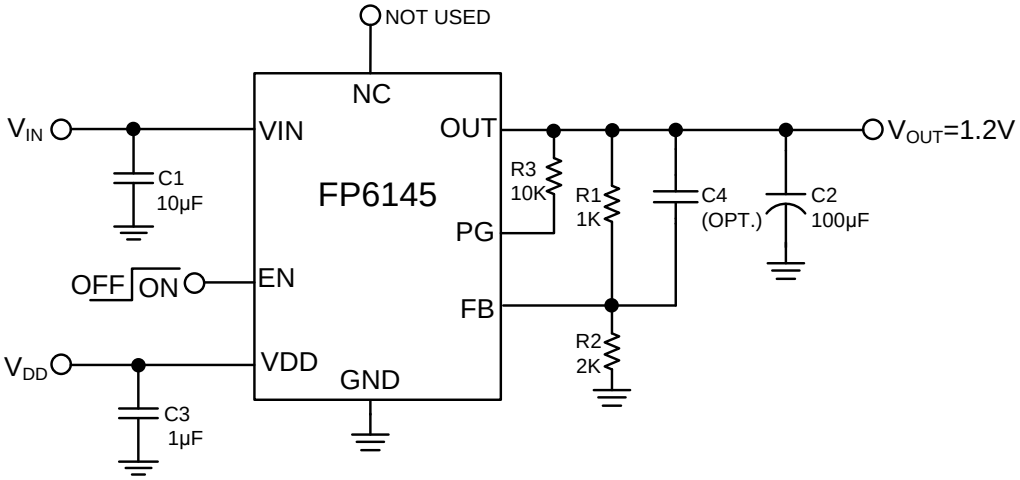


Figure 2. Typical Application Circuit

Functional Pin Description

I/O	Pin Name	Pin No. (SOP-8EP)	Pin No. (TDFN-10L)	Pin Function
O	PG	1	5	Power good output pin.
I	EN	2	6	On/Off control input. Drive EN above 1.2V to turn the device on, and drive EN below 0.4V to turn the device off.
I	VIN	3	7, 8, 9	MOSFET power supply pin.
I	VDD	4	10	Power input for controller including error amplifier, reference and other protect circuits.
O	NC	5	-	No connection.
O	OUT	6	1, 2, 3	Regulated voltage output.
I	FB	7	4	Voltage feedback input pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.8V.
I	GND	8, 9	11	Ground pin. Connect GND to exposed pad.

Block Diagram

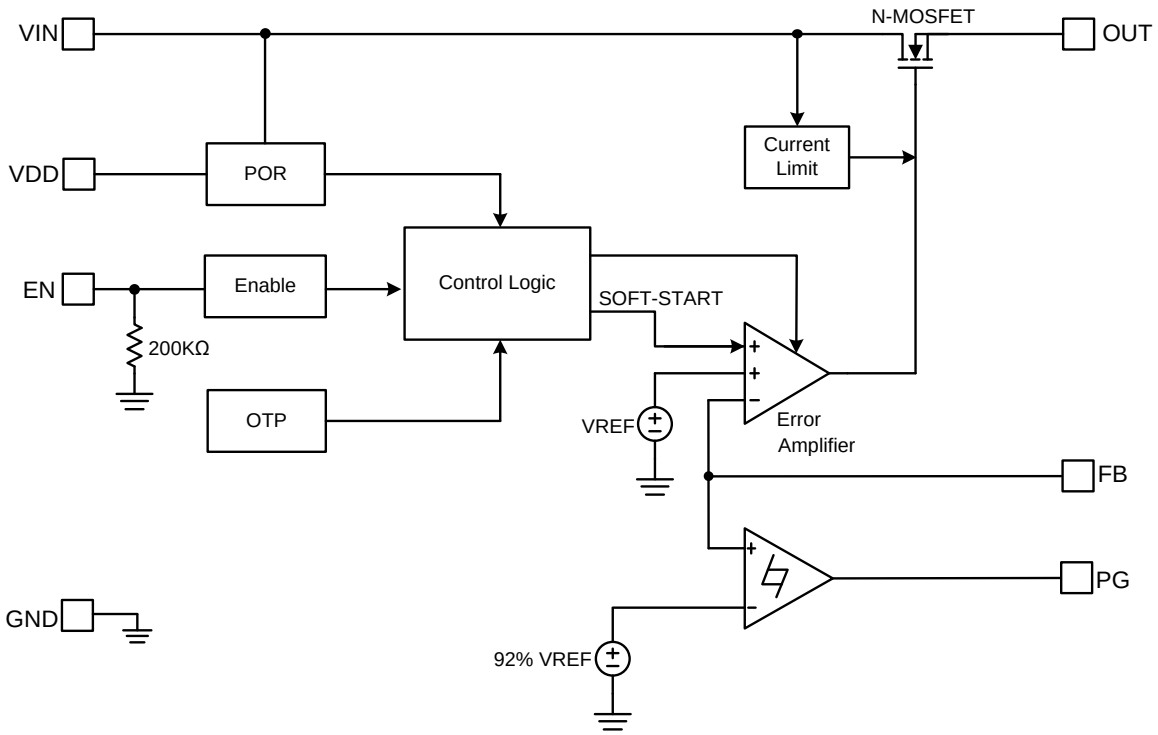


Figure 3. Block Diagram of FP6145

Absolute Maximum Ratings

- VDD Supply Voltage ---------- -0.3V to +6.5V
- Supply Voltage (VIN) ---------- -0.3V to +6.5V
- EN and FB Pin Voltage ---------- -0.3V to V_{DD}+0.3V
- Power good Voltage ---------- -0.3V to +6.5V
- Power Dissipation @T_J=150°C, T_A=25°C (P_D)
  - SOP-8 (Exposed Pad) ---------- 2.08W
  - TDFN-10L (3mmx3mm)---------- 1.79W
- Package Thermal Resistance (θ_{JA}) (Note 1)
  - SOP-8 (Exposed Pad) ---------- 60°C/W
  - TDFN-10L (3mmx3mm)---------- 70°C/W
- Package Thermal Resistance (θ_{JC})
  - SOP-8 (Exposed Pad) ---------- 15°C/W
  - TDFN-10L (3mmx3mm)---------- 30°C/W
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Junction Temperature (T_J) ---------- -40°C to +150°C
- Storage Temperature (T_{STG}) ---------- -65°C to +150°C

Note1: θ_{JA} is measured with the PCB copper area (need connect to Exposed-Pad) of approximately 1.5 in^2 (Multi-layer).

Recommended Operating Conditions

- VDD Supply Voltage ---------- +3V to +5.5V
- VIN Supply Voltage (Conditions: $V_{IN} \leqq V_{DD}$) ---------- +1.2V to +5.5V
- Output Voltage (Conditions: V_{DD}-V_{OUT}>1.9V) ---------- +0.8V to V_{IN}-V_{DROP}
- Output Current ---------- 0A to 3A
- Operating Ambient Temperature Range ---------- -40°C to +85°C
- Operating Junction Temperature Range ---------- -40°C to +125°C

Electrical Characteristics (Note 2)

(V_{DD}=5V, V_{IN}=1.5V, V_{OUT}=1.2V, T_A=25°C unless otherwise specified)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Units
VDD POR Threshold		V_{DD}			2.5	2.7	2.9	V
VDD POR Hysteresis (Note 3)		$V_{DD\ (hys)}$			-	0.4	-	V
VIN POR Threshold		V_{IN}			0.95	1.05	1.15	V
VIN POR Hysteresis (Note 3)		$V_{IN(hys)}$			-	0.3	-	V
VDD Nominal Supply Current		I_{DD}	EN=V_{DD}		-	1	1.2	mA
VDD Shutdown Current		I_{SD}	EN=0V		-	5	10	μA
Feedback Voltage		V_{FB}	V_{DD}=3.0V~5.5V I_{OUT}=10mA		0.79	0.8	0.81	V
Load Regulation			I_{OUT}=0A~3A		-	0.5	1	%
Dropout Voltage		V_{DROP}	I_{OUT}=3A V_{DD}=5V	1.2V＜V_{OUT}＜1.8V	-	0.23	0.28	V
				1.8V≦V_{OUT}＜2.5V	-	0.24	0.29	
				2.5V≦V_{OUT}≦2.8V	-	0.28	0.38	
VOUT Pull Low Resistance			EN=0V		-	85	-	Ω
Soft Start Time		T_{SS}			-	2	-	mS
EN Pin Logic High Threshold Voltage		V_{ENH}	Enable		1.2	-	-	V
		V_{ENL}	Disable		-	-	0.4	
EN Pin Pull Low Resistor		R_{EN}			-	200	-	KΩ
Current Limit		I_{LIM}	V_{DD}=3V~5.5V		4	5	-	A
Ripple Rejection	VIN	PSRR	F=120Hz, I_{OUT}=100mA		-	65	-	dB
	VDD				-	65	-	
Under-Voltage Threshold			V_{FB} Falling		-	0.35	-	V
Under-Voltage Protect Current Foldback					-	120	-	mA
PG Threshold Voltage		V_{PG}	V_{FB} Rising, V_{OUT}=V_{FB}		89	92	95	%V_{FB}
PG Threshold Hysteresis		$V_{PG(HYS)}$	V_{FB} Falling, V_{OUT}=V_{FB}			3		%V_{FB}
PG Low Voltage			PG Sinks 5mA		-	0.25	0.4	V
Thermal shutdown Temperature		TSD			-	170	-	°C
Thermal Shutdown Hysteresis					-	50	-	°C

Note2: V_{IN}≦V_{DD} is required in all applications.
Note3: Guarantee by design.

Typical Performance Curves

V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2, I_{OUT}=0A

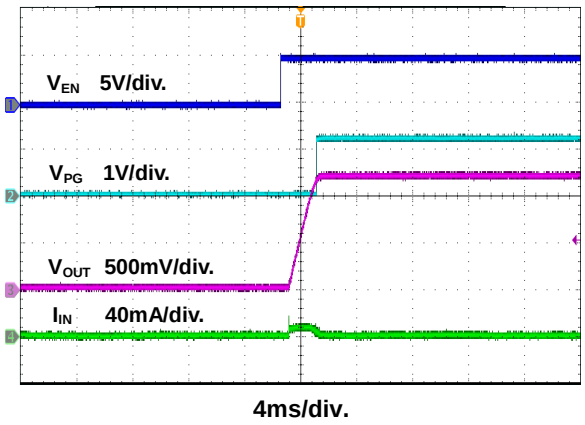


Figure 4. EN Turn ON Waveform

V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2, I_{OUT}=3A

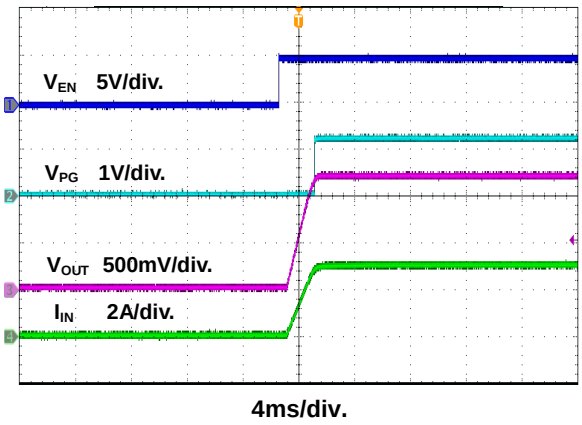


Figure 5. EN Turn ON Waveform

V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2, I_{OUT}=0A

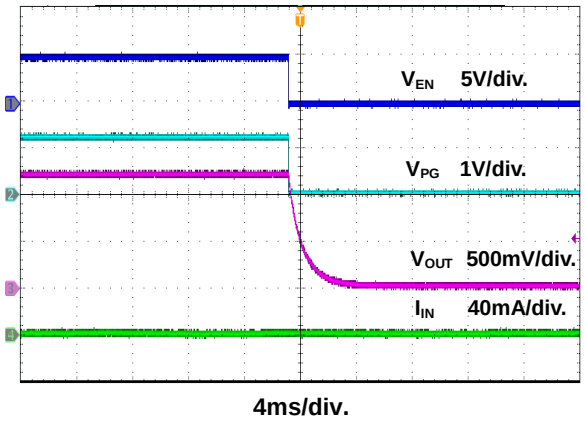


Figure 6. EN Turn OFF Waveform

V_{CNTL}=5V, V_{IN}=1.5V, V_{OUT}=1.2, I_{OUT}=3A

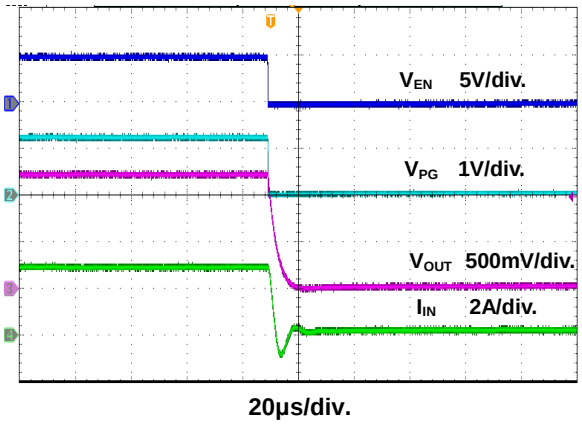


Figure 7. EN Turn OFF Waveform

V_{IN}=V_{CNTL}= V_{EN}=3.3V, I_{OUT}=0A→3A→0A

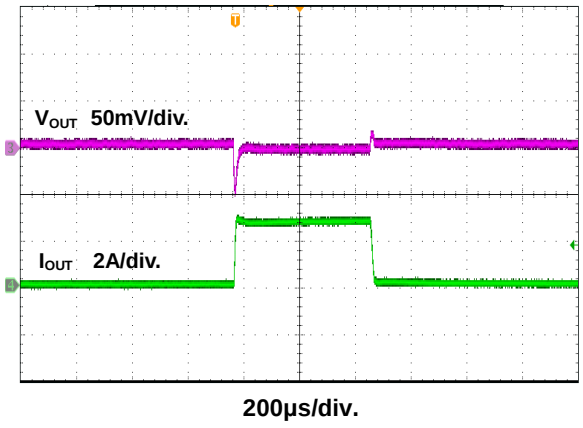


Figure 8. Load Transient Response

V_{CNTL}= V_{EN}=5V, V_{IN}=1.5V, I_{OUT}=0A→3A→0A

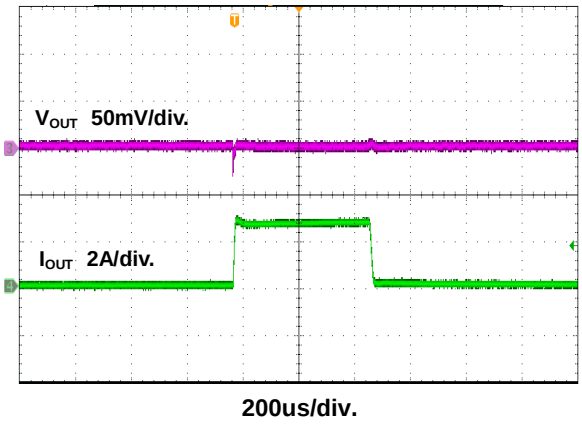


Figure 9. Load Transient Response

Typical Performance Curves (Continued)

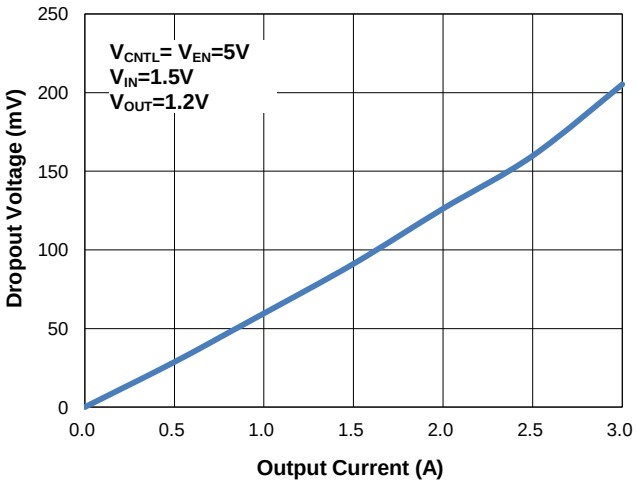


Figure 10. Dropout Voltage vs. Output Current

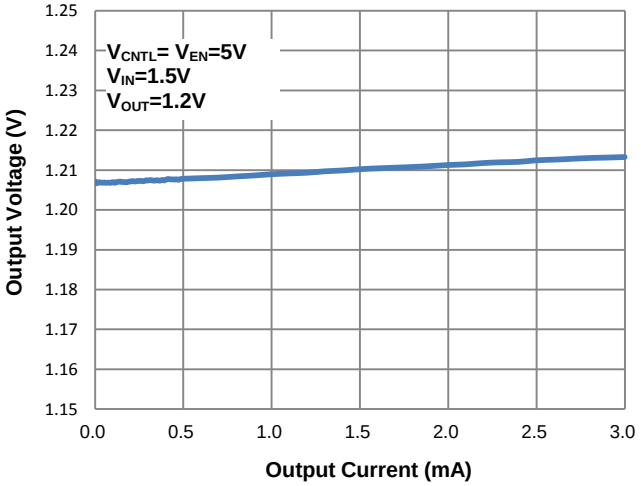


Figure 11. Output Voltage vs. Output Current

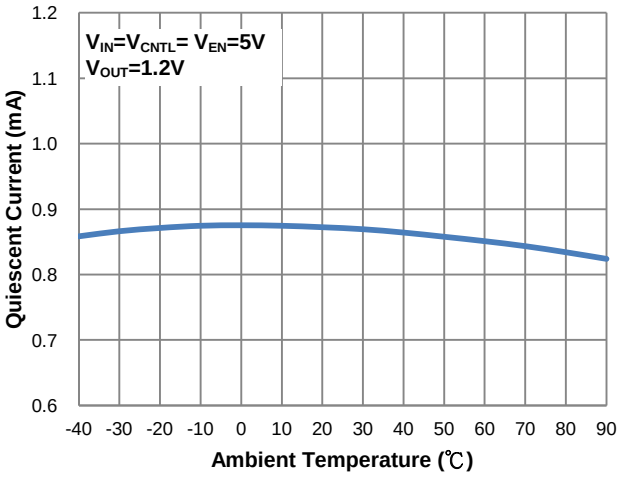


Figure 12. Quiescent Current vs. Ambient Temperature

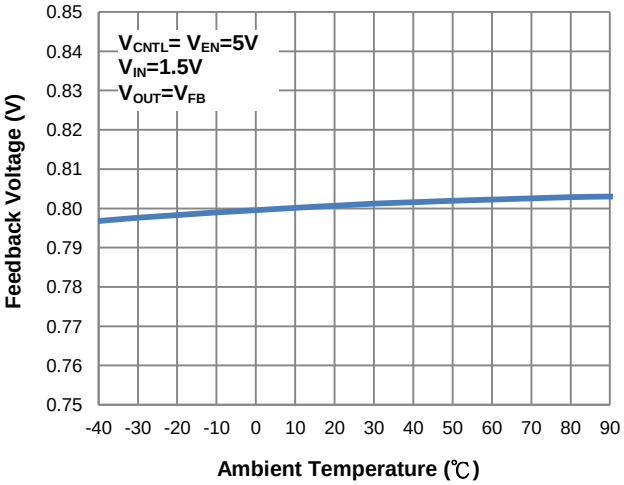


Figure 13. Feedback Voltage vs. Ambient Temperature

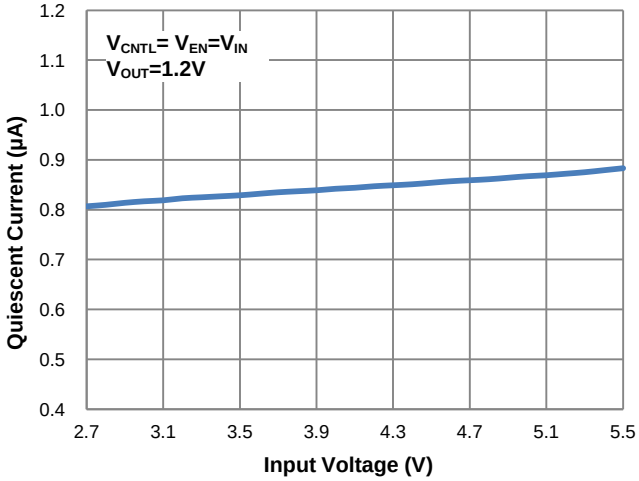


Figure 14. Quiescent Current vs. Input Voltage

Functional Description

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT}=0.8V\times\left(1+\frac{R1}{R2}\right)$$

Where R1 is connected from V_{OUT} to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected with R1 in parallel to improve load transient response. The recommended R2 and R1 are in the range of 1K~100KΩ.

VIN

Main supply input pin for power conversions. The voltage at this pin is monitored for Power-On Reset purpose.

VDD

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

PG

Power Good signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin will be pulled low when the rising FB voltage is not above the VPG threshold or the falling FB voltage is below the VPG threshold, indicating the output is not OK.

EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle.

VOUT

Output of the regulator. Please connect Pin 3 and Pin 4 with wide tracks. It is necessary to connect an output capacitor with this pin for closed-loop compensation and improving transient responses.

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VDD and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the PG pin regardless the output voltage when the VDD voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2mS.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to preset voltage. The error amplifier designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from V_{IN} to V_{OUT}.

Current-Limit

The FP6145 monitors the current via the output NMOS and limits the maximum current to prevent load and FP6145 from damages during overloading or short circuit conditions.

Under-Voltage Protection (UVP)

The FP6145 monitors the voltage on FB pin after soft-start process finished. Therefore the UVP is disabling during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit will shut off the output immediately. After a while, the FP6145 will start a new soft-start to regulate output.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of FP6145. When the junction temperature exceeds +170°C, a thermal sensor will turn off the output NMOS and allow the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools 50°C, resulting in a pulsed output during continuous thermal overload conditions.

Application Information

Input Capacitor

A minimum 1μF input ceramic capacitor is required. X5R or X7R is recommended. The capacitor should be placed as close to the device as possible for optimal performance.

Output Capacitor

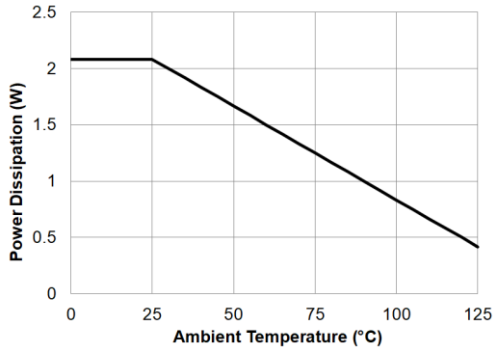
The FP6145 requires a minimum of output capacitor to maintain stability. The FP6145 is designed to be stable with low ESR ceramic capacitor. A 10μF ceramic capacitor is sufficient for most applications. X5R or X7R is recommended. The output capacitor must be placed within 1cm from the output pin of the device.

Thermal Considerations

The power dissipation of the device can be determined with the formula:

$$P_D \approx (V_{IN}-V_{OUT}) \times I_{OUT}$$

Additional copper area for heat sink is required in applications where the minimum input voltage is known and is large compared with the dropout voltage. The below figure shows the maximum allowable power dissipation of SOP-8 exposed pad package for different ambient temperatures, assuming θ_{JA} is 60°C/W and the maximum junction temperature is 125°C.

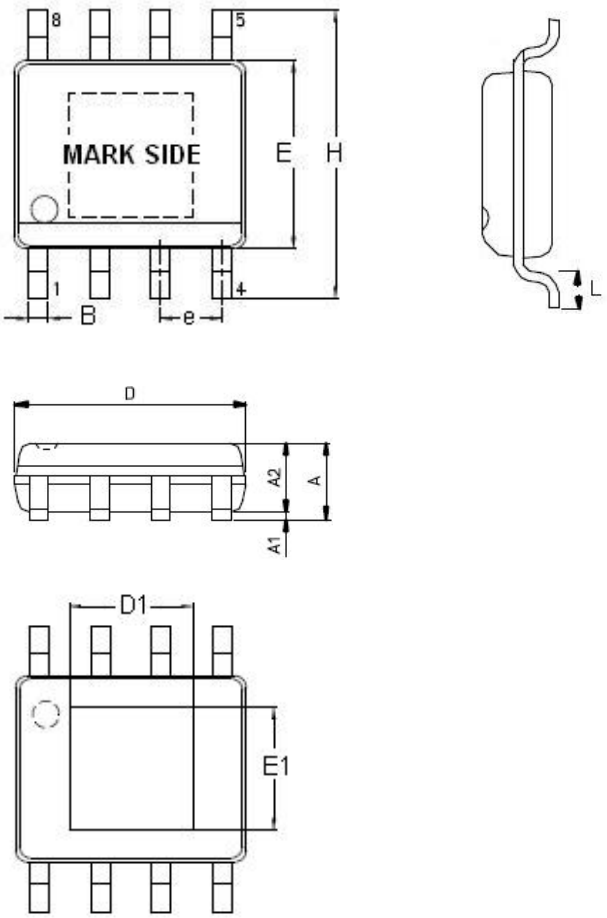


PCB Layout Consideration

1. Place the input capacitors of VIN and VDD as close to the device as possible.
2. Place output capacitor as close to the device as possible.
3. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. The area should be maximized to improve thermal performance.
4. Place R1, R2 and C4 close to the device to avoid noise coupling.
5. Use wide tracks for large current paths.

Outline Information

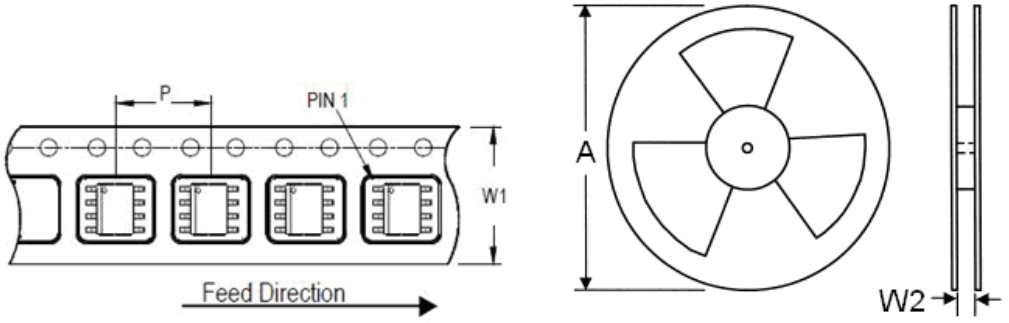
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note4: Followed From JEDEC MO-012-E.

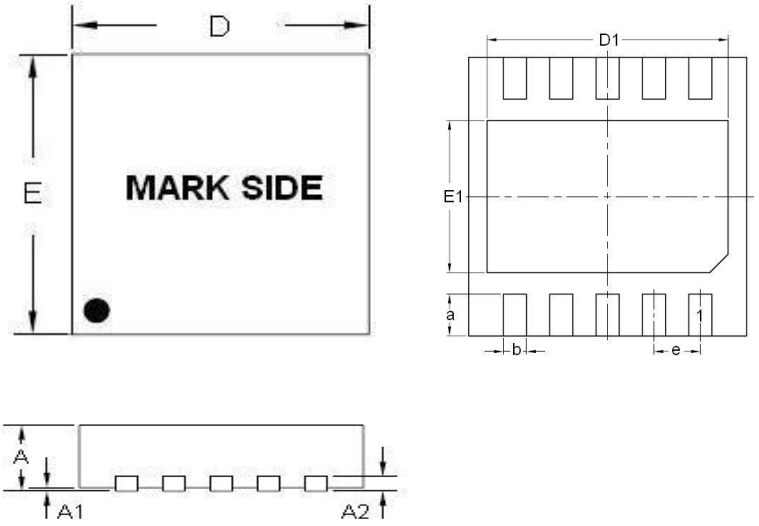
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

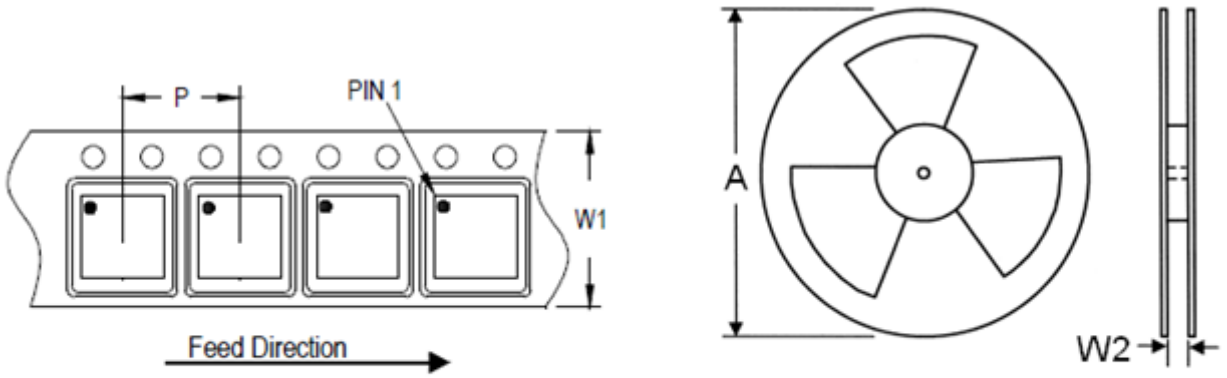
Outline Information (Continued)

TDFN-10L (3mmx3mm) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	2.95	3.05
E	2.95	3.05
a	0.30	0.50
b	0.18	0.30
e	0.45	0.55
D1	2.20	2.70
E1	1.40	1.75

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000